PRIMARY BLOCK DIAGRAM
LONG ADD

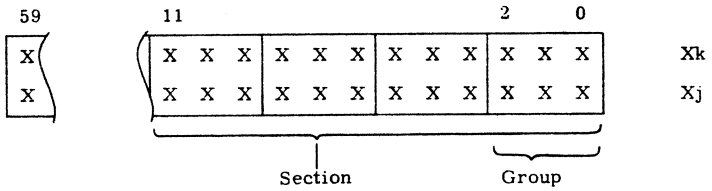
The Long Add Unit executes CPU instructions 36 and 37. It performs a 60-bit integer addition to X Register operands specified by the j and k portions of the instruction and delivers the 60-bit sum to the X Register specified by the i portion of the instruction. Prior to addition, the unit complements the Xk and Xj operands for the 36 instruction (Integer Sum) and only the Xj operand for the 37 instruction (Integer Difference).

The long add instructions require two clock periods for execution. The operands move from the X Registers to the Long Add Unit in the same clock period in which the instruction issues from the CIW Register. The result moves from the Long Add Unit to the destination X Register during the following clock period. A new instruction may issue from the CIW Register for execution in the Long Add Unit each clock period.

OPERATION

The Long Add Unit complements the operands as specified by the instruction code and forms a partial sum in the first stage of addition. The partial sum enters the second stage of the adder where the resultant sum is formed from the partial sum. At this point the resultant sum is in ones complement form. The Go Long Add flag, sent from the CPU, gates this sum to the result X Register through a static network which complements it to return it to true form.

Adder Format



FIRST STAGE

The first stage of addition forms a partial sum which consists of Bit Enables, Bit Borrow Generates, Group Borrow Generates, Section Borrow Generates and Section Enables. Group Enables are also generated but are not sent to the second stage of the adder.

$$\text{Bit Enables} = \overline{0 \cdot 1} \;\text{OR}\; \overline{1 \cdot 0}$$

$$= \overline{E} \;\text{OR}\; \overline{E}$$

Bit Borrow Generates = $\frac{1}{\overline{B}}$

Group Borrow Generates = Borrow out of 3 bit group.

Example: 110 OR 010 = 000 OR 101 OR 110 = 011 etc.

Group Enable = All Bit Enables in group equal to one.
Section Borrow Generates = Borrow out of 12 bit section.
Section Enable = All Group Enables in section equal to one.

SECOND STAGE

The second stage of the adder forms Group Borrow Inputs and Bit Borrow Inputs from the partial sum. An EXCLUSIVE OR of the Bit Borrow Inputs and the Bit Enables forms the sum. The sum at this point is in ones complement form.

Group Borrow Inputs = Borrow into the group

Bit Borrow Inputs = Borrow into bit

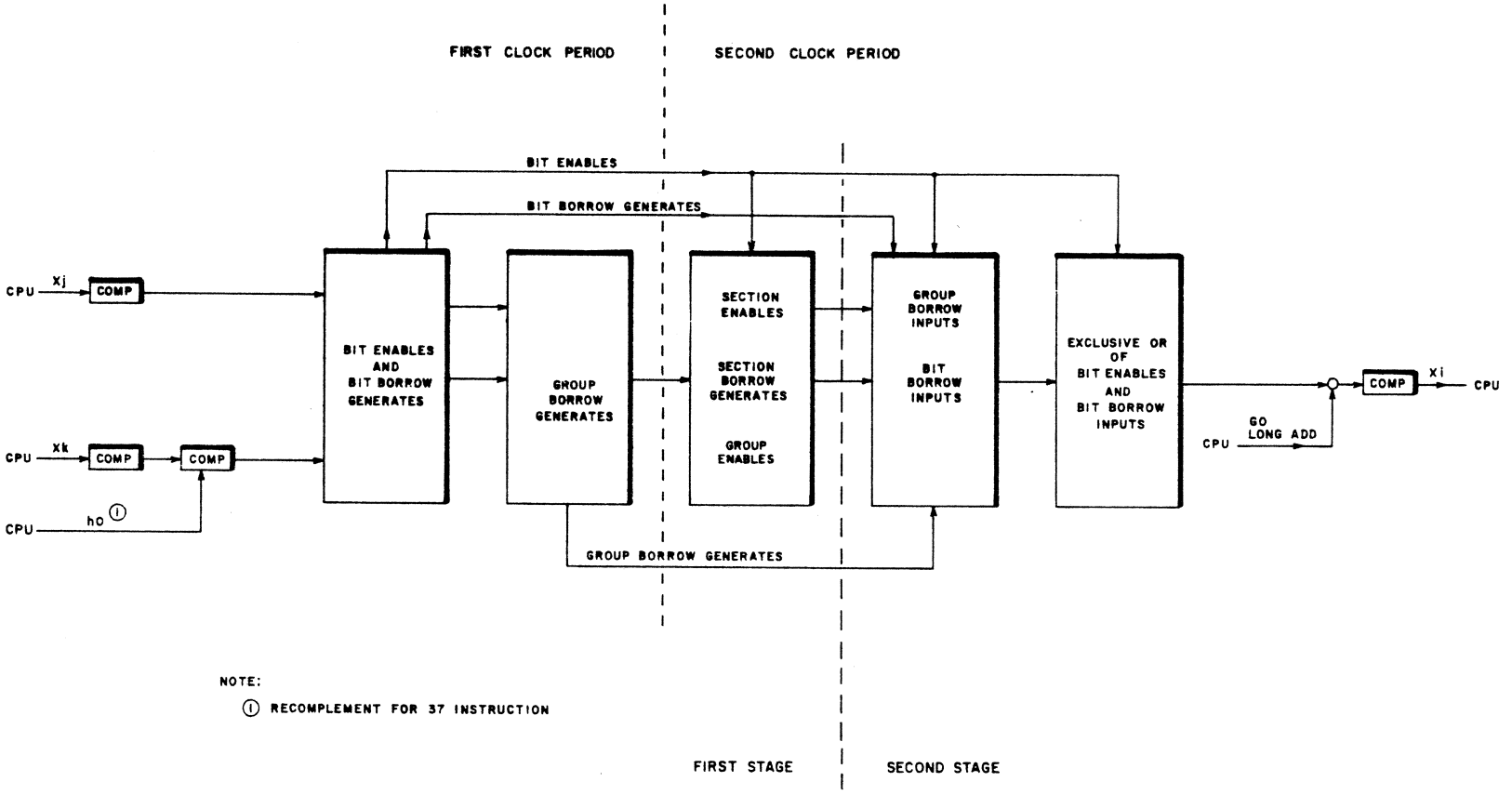
Example:

The following is an example using a 12-bit adder performing a 36 instruction. In this case the Section Borrow Generate is the end around borrow. In the case of the Long Add Unit it is the Section Borrow from the highest order section.

36 Instruction Example:

4470_8 → COMP → 3307_8 → 011 011 000 111
1532_8 → COMP → 6245_8 → 110 010 100 101
6222_8

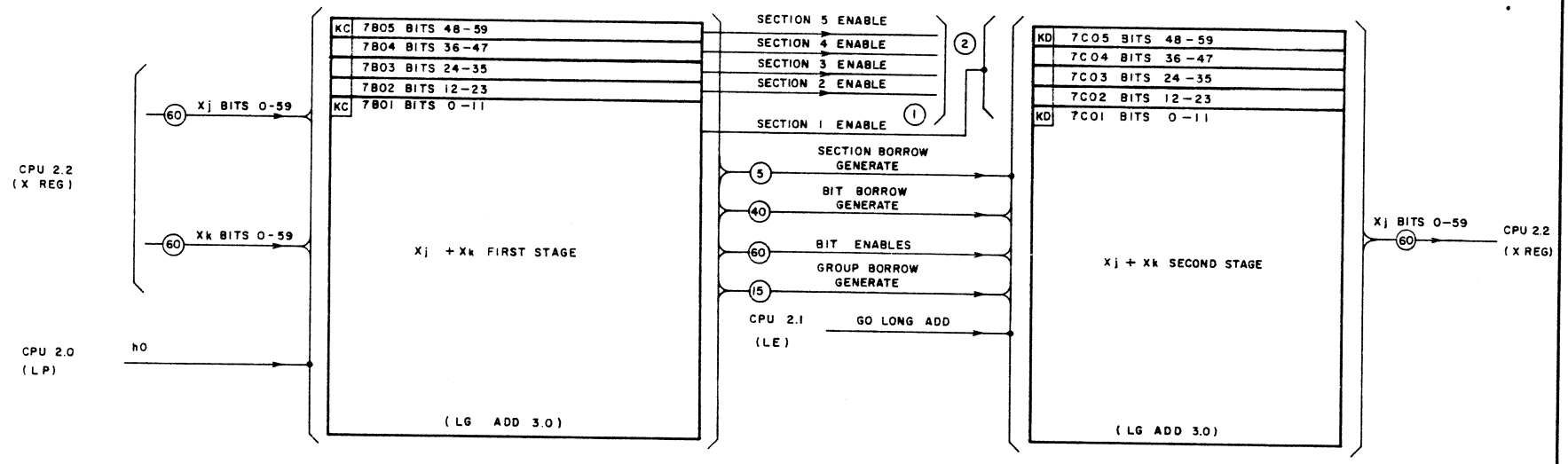
101	001	100	010	BIT ENABLES
010	010	000	101	BIT BORROW GENERATES
1	0	0	1	GROUP BORROWS GENERATES
1				SECTION BORROW GENERATES
0				SECTION ENABLE
0	0	1	1	GROUP BORROW INPUTS
100	100	001	111	BIT BORROW INPUTS
001	101	101	101	EXCLUSIVE OR OF BIT BORROW INPUTS and BIT ENABLES
110	010	010	010	COMPLEMENTED
6	2	2	2_8	



NOTE:

① RECOMPLEMENT FOR 37 INSTRUCTION

CONTROL DATA	PRIMARY BLOCK DIAGRAM	CODE IDENT	DWG NO	REV
DEVELOPMENT DIVISION	LONG ADD	34010	60348000	A
		C	SHEET LG ADD10	PAGE 5-10-1



NOTE :

(1) SECTION 1 ENABLE GOES TO 7C02, 7C03, 7C04, 7C05

(2) SECTION 2 ENABLE GOES TO 7C01, 7C03, 7C04, 7C05

SECTION 3 ENABLE GOES TO 7C01, 7C02, 7C04, 7C05

SECTION 4 ENABLE GOES TO 7C01, 7C02, 7C03 7C05

SECTION 5 ENABLE GOES TO 7C01, 7C02, 7C03, 7C04

CONTROL DATA DEVELOPMENT DIVISION	SECONDARY BLOCK DIAGRAM LONG ADD	CODE IDENT 34010	DWG NO 60348000	REV A
		SIZE C	SHEET LG ADD 2.0	PAGE 5-10-3

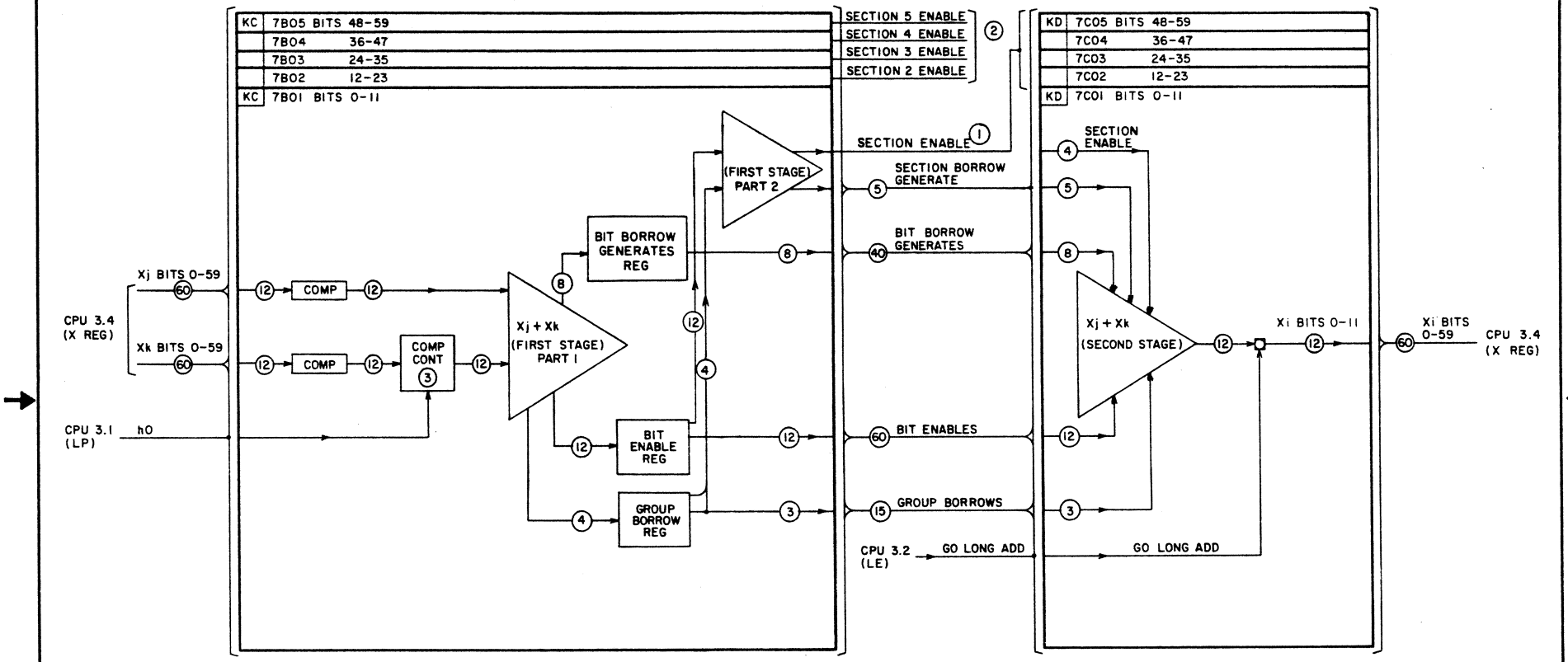
The Long Add Unit executes CPU instructions 36 and 37. It performs a 60-bit integer addition to X Register operands specified by the j and k portions of the instruction and delivers the 60-bit sum to the X Register specified by the i portion of the instruction. Prior to addition, the unit complements the Xk and Xj operands for the 36 instruction (Integer Sum) and only the Xj operands for the 37 instruction (Integer Difference).

The long add instructions require two clock periods for execution. The operands move from the X Registers to the Long Add Unit in the same clock period in which the instruction issues from the CIW Register. The result moves from the Long Add Unit to the destination X Register during the following clock period. A new instruction may issue from the CIW Register for execution in the Long Add Unit each clock period.

During the first clock period the KC modules complement both operands. If the instruction is Integer Difference (37), h0 will be equal to one and the KC modules recomplement the Xk operand. After the complementing the operands enter the first stage of the adder.

The first stage of the adder in the Long Add Unit is divided into two parts. The first part forms the Bit Enables, Bit Borrow Generates and Group Borrow Generates. Registers hold them for use during the second clock period. The second part of the first stage of addition takes place during the second clock period. It consists of forming Section Borrow Generates and Section Enables.

The KC modules send the partial sum to the KD modules where the second stage of addition takes place. Go Long Add gates the resultant sum from the second stage through an AND NOT to the result X Register.



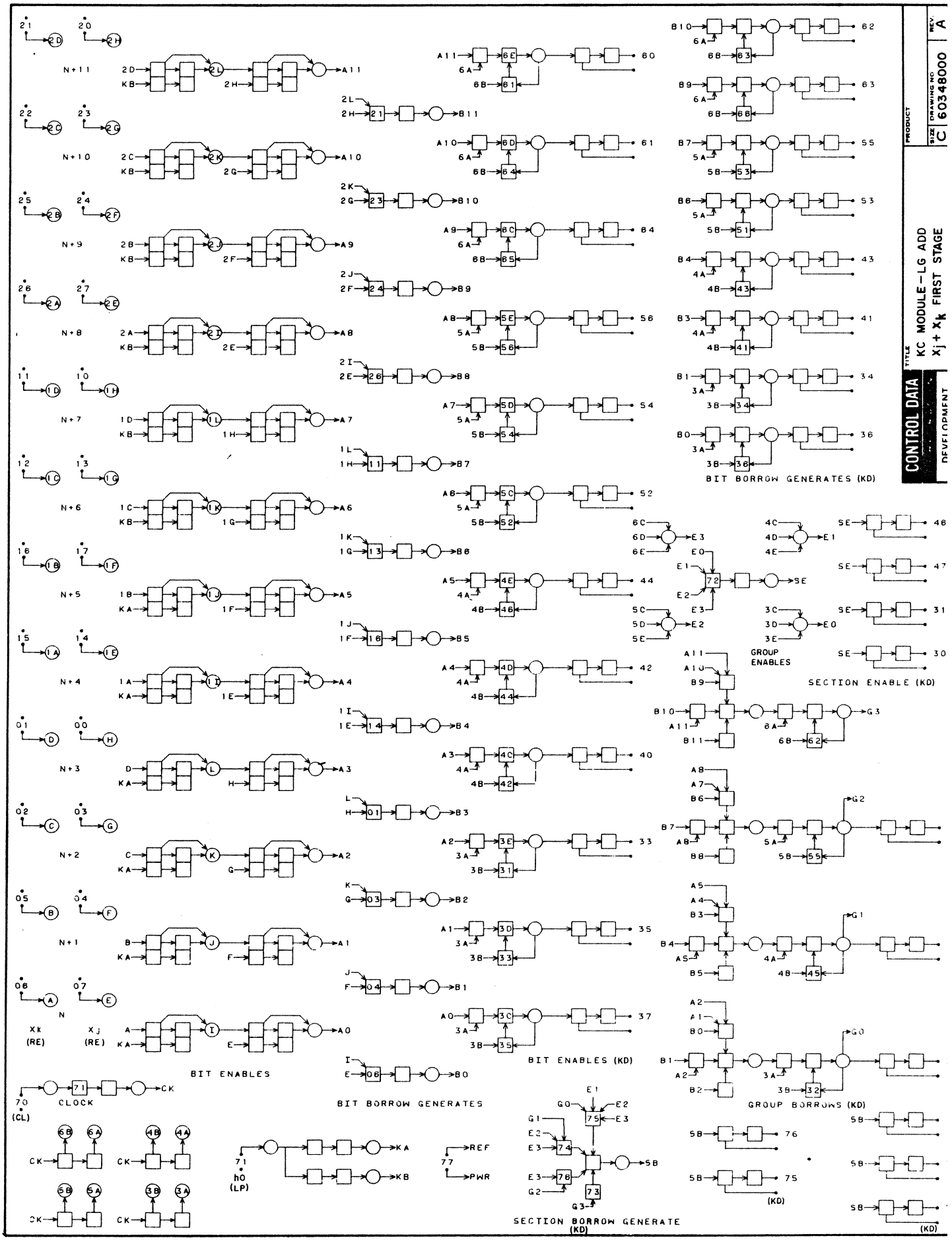
NOTE:

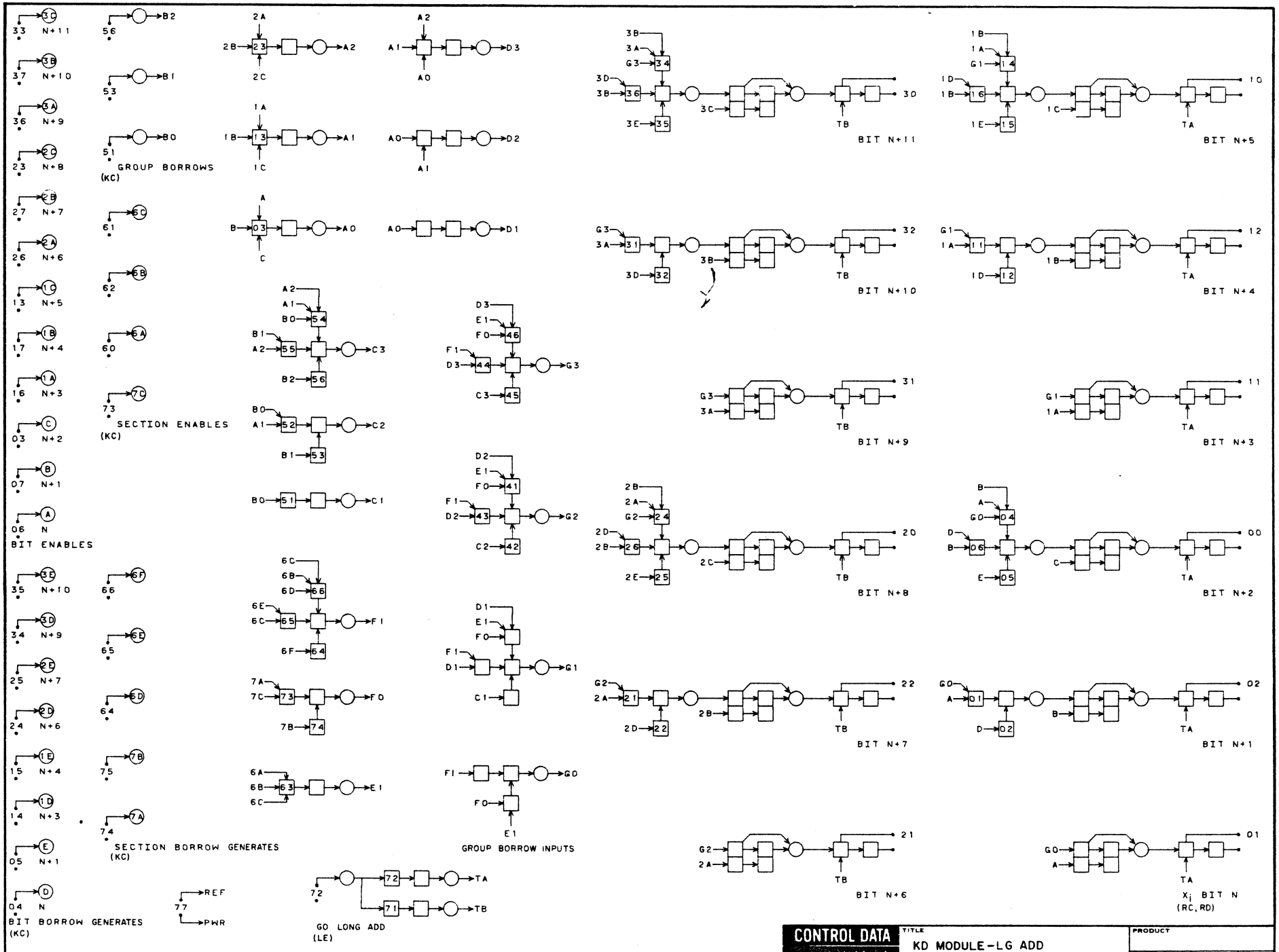
(1) SECTION 1 ENABLE GOES TO 7C02, 7C03, 7C04, 7C05

(2) SECTION 2 ENABLE GOES TO 7C01, 7C03, 7C04, 7C05
SECTION 3 ENABLE GOES TO 7C01, 7C02, 7C04, 7C05
SECTION 4 ENABLE GOES TO 7C01, 7C02, 7C03, 7C05
SECTION 5 ENABLE GOES TO 7C01, 7C02, 7C03, 7C04

(3) h0=1 RECOMPLEMENT Xk OPERAND

CONTROL DATA					
DEVELOPMENT DIVISION	DETAILED-MODULES DIAGRAM LONG ADD	CODE IDENT 34010	DWG NO 60348000	REV A
		C	SHEET LG ADD30	PAGE 5-10-5


BIT BORROW GENERATES (KD)
BIT ENABLES
BIT BORROW GENERATES
BIT ENABLES (KD)
GROUP ENABLES
SECTION ENABLE (KD)
GROUP BORROWS (KD)
SECTION BORROW GENERATE (KD)
CLOCK
CONTROL DATA
DEVELOPMENT
KC MODULE-LG ADD
$X_j + X_k$ FIRST STAGE
PRODUCT
SIZE C
DRAWING NO 60348000
REV A


BIT ENABLES
SECTION ENABLES (KC)
GROUP BORROWS (KC)
SECTION BORROW GENERATES (KC)
BIT BORROW GENERATES (KC)
GROUP BORROW INPUTS
GO LONG ADD (LE)
BIT N+11
BIT N+10
BIT N+9
BIT N+8
BIT N+7
BIT N+6
BIT N+5
BIT N+4
BIT N+3
BIT N+2
BIT N+1
Xi BIT N (RC, RD)
CONTROL DATA
KD MODULE-LG ADD
Xj + Xk SECOND STAGE
PRODUCT
SIZE C
DRAWING NO 60348000
REV A