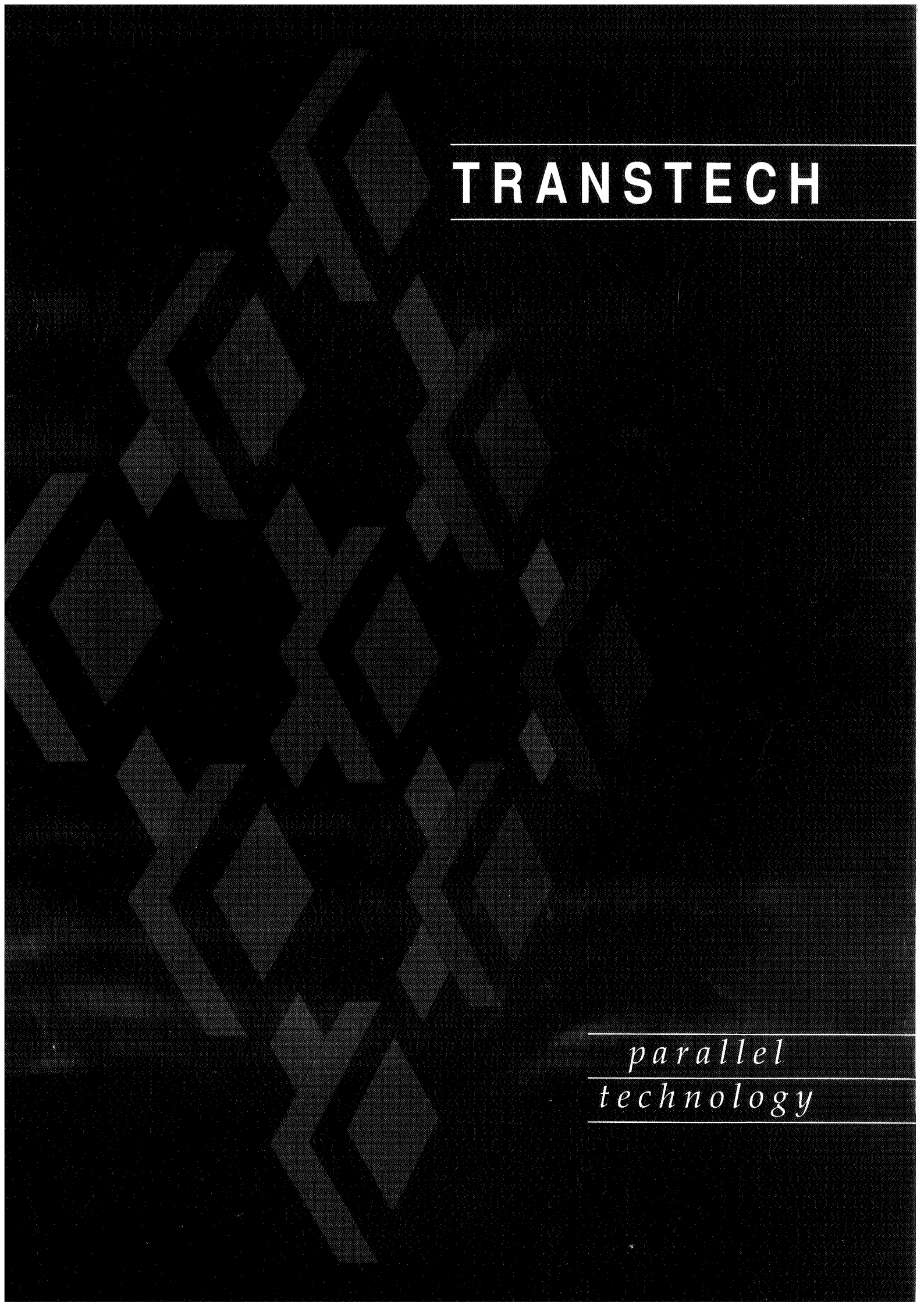
Transputer: Transtech


TRANSTECH
parallel
technology

THE PARALLEL PROCESSING BUSINESS

The last decade has seen the emergence of parallel processing as an accessible technology. Creating the ability to resolve computationally intensive problems, by splitting and spreading the load across banks of communicating processors, led to the development of RISC and array processors, and on to transputers. These silicon solutions allowed the cost of processing power to fall dramatically, 100 MIPs or more on an IBM PC plug-in board. Having brought super-computer power to the desk top, parallel processing had ensured its inevitable route to acceptability.

The applications in business and industry now stretch from dealing systems in the financial world, via video telecommunications, graphic systems satisfying film industry requirements, to flight control systems. The challenge is to ensure that Open System Standards, now accepted world wide, are applied to parallel processing; only then will the increasingly mature areas of application accept and use this power within and alongside current commercial and industrial systems.

Operating as the commercial and technical interface to the users and developers of parallel processing applications calls for an unusual combination of skills. It requires a team that is as comfortable with silicon advances as with new operating systems, people who can customise turnkey solutions for commercial applications as easily as they specify and develop parallel processing kernels.

The TRANSTECH Group is successfully fulfilling this role; it has the expertise, the resource and the experience.

It is the total solution vendor for parallel processing.

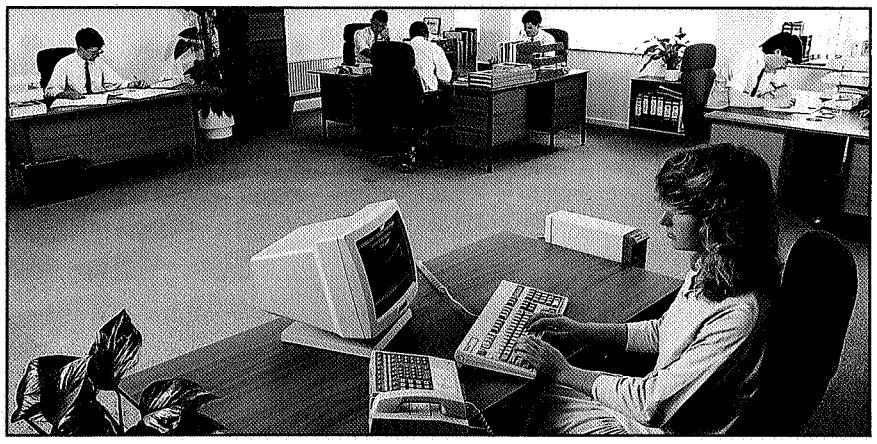
HEADQUARTERS HIGH WYCOMBE UK

THE COMPANY

Transtech was formed in March 1986 initially as the research, government establishment and education agent for INMOS transputer based products. The portfolio was quickly expanded, to include systems from the key parallel processing start-ups. Commitment to customer support and service, backed by an expert technical team, has driven Transtech's growth and it is now recognised as Europe's leading transputer supplier. Already a major manufacturer, Transtech has led the development of open systems for both parallel processing hardware and software; this proven on a growing family of host environments.

FACILITIES

Expanding into an international group, the headquarters of the operation is a modern facility, red brick, 4000 sq.ft. and equipped to support the planned growth. It is well located being a few minutes from the centre of High Wycombe, Buckinghamshire, giving easy access to the key industrial and technology zones, and to Heathrow Airport. This ensures fast and easy access to customers throughout the world, as well as within the UK.



SALES AND SERVICE

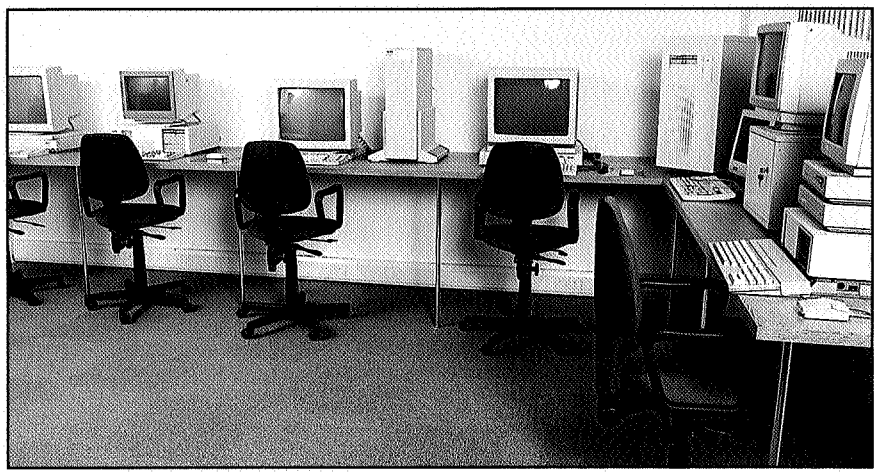
Transtech has built dedicated sales and customer service teams, these being experienced people in both the commercial and technical requirements of supporting high performance systems. Combining these skills with a well developed contact and information database has given much to Transtech's reputation for satisfying customer demand.

Efficient stock control and shipment expertise that is world-wide are further evidence that Transtech can deliver solutions, when they are needed.

Quality assurance is a crucial element, all products having a 24-hour Burn In before allocation to stock, and then each product is again functionally tested prior to customer shipment. Full hardware and software warranties are given, with maintenance contracts available across the complete range of products; these are supported by the service department. It is fully equipped and trained to deal with the wide range of systems and hosts supported, the aim being a 24 hour turn round. A necessary part of success as a total solution vendor.

TECHNICAL SUPPORT

Nobody can seriously operate in the parallel processing market without a highly skilled and experienced applications team. Transtech's team of graduate engineers are actively working with customers to develop parallel processing applications. The same engineers are responsible for systems integration, with access to the hardware and system software development engineers; responsibility further extends to on-site installation, ensuring continuous involvement.



Headquarters has an extensive demonstration suite, with the current systems and hosts available. The applications and sales teams are able to configure systems to customers requirements and compare solutions built on a variety of hosts. All part of the commitment to total support from one vendor.

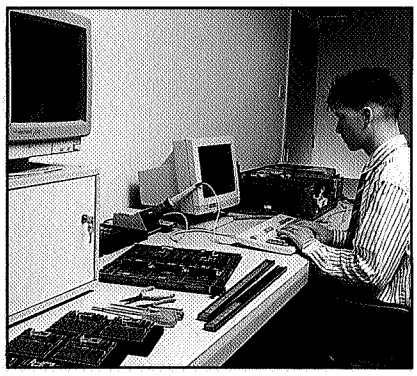
Training is vital to bringing new technology on stream quickly, both within a customer's operation and at Transtech. The training facility is excellent, it holds over 30 in comfort and contains all the aids necessary, including a full disc to screen presentation system.

Transtech's combination of experienced engineers supported by excellent facilities for demonstration and training is essential to the proper support of high performance systems.

DEVELOPMENT AND MANUFACTURING

The entry of Transtech into design and manufacture came soon after starting business, and this has evolved into two leading teams developing the range of parallel processing systems.

Hardware has embraced the motherboard/daughterboard concept, bringing product to market from simple plug-ins for standard PCs to fully configured systems based on high performance engineering workstations. These products are among the most advanced available with superb quality of design, performance and reliability; they lead the development of open system parallel processing. This team has been designing parallel system products since the first availability of silicon, some members having been intimately involved in its evolution.



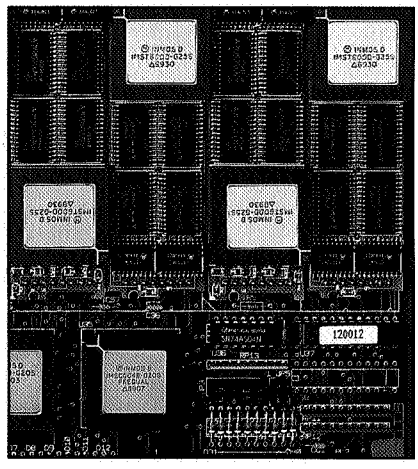
In parallel, the software team's output of both operating systems and support routines fully utilises the power and flexibility offered by the range of host/hardware options. The core of this team was responsible for the first clean interface between UNIX and parallel processors.

Both teams are fully supported with access to all the current host systems and with facilities to configure test and support all the product in development. The schedule of product advances is based on Transtech's commitment to leading the open system expansion of parallel processing.

With manufacture under direct control, new systems and improvements can quickly be assimilated into the range. The feedback from customers, added to market forecast, ensures that the business is controlled to the customers benefit and thus allows the latest specifications to be properly integrated and in a timely manner. The range is built and tested alongside the host systems, ensuring that quality and reliability match the environment within which it has to operate.

CONSULTANCY

Combining the skill base of the Transtech teams gives an unequalled capacity for providing consultancy. Not only can advice be given on systems specification, but on suitability, application and training, all with a range of options and none causing commitment to a closed system. The client will be able to embrace industry standards and match these to his processing need.

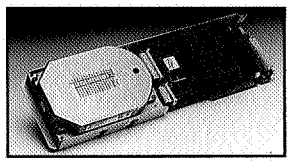


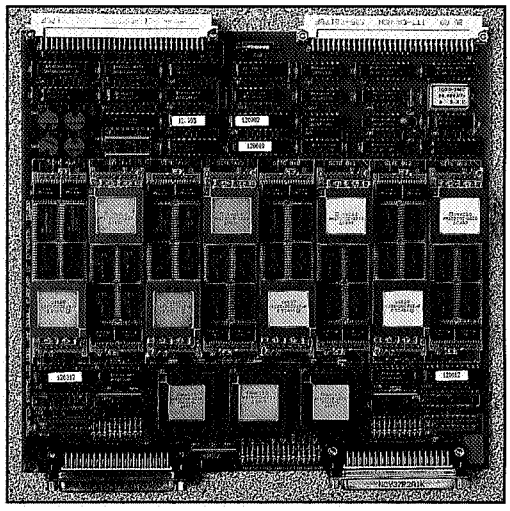
This dedication to customer problem solving, coupled with the commitment to open systems, has lead to Transtech's emergence as the leading supplier of parallel processing solutions.

THE PARALLEL ENVIRONMENT

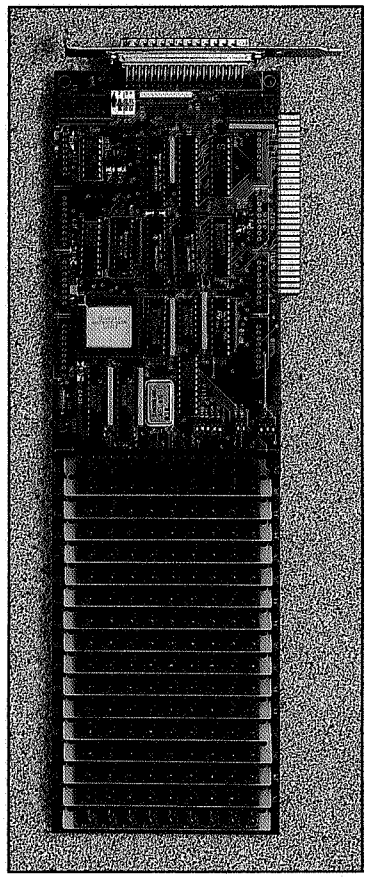
With parallel processors interfaced to a number of host machines, the goal is to create environments where the systems operate cleanly within the industry standards used by the main hosts (PC AT, Sun, HP, VME etc.).

Such a scenario demands that a range of options allows expandability where necessary, as parallel processing calls for variable numbers of processors as an application gets developed or processing power increases. The software environment which can allow such reconfiguration but within standard operating systems, has been enhanced by Transtech and is the key to true open systems.





The natural base for development systems was the PC AT family, and it was from there that applications first evolved. This has lead to new standards of host machine, utilising the performance and operating systems of the sophisticated workstations now available. This equipment includes the offerings from Sun, Hewlett Packard, Apollo and Apple. Similar applications have evolved for industrial standards like VME and Eurocard, which utilise the software standards set by the major systems.



The philosophy behind the availability of such a wide range of host machines is that of small standardised daughter boards married to motherboards targeted at each host. Both types of board can be highly functional, offering a wide range of application specific interfaces and processing/memory options. Extending this philosophy to the communication, protocol and instrumentation standards is now the main challenge.

To further this Transtech has developed a generic system environment, GENESYS, a parallel run time package operating seamlessly on top of UNIX. It is intended to be both host and processor independent.

Combined with the development of simplified installation packages and the attention to ensuring functionality, the total support approach of Transtech has brought integrated solutions to the evolving parallel processing market.

HARDWARE FAMILIES

The basic daughterboard / motherboard design is based on the initial transputer modules, or TRAMs. The first TRAMs containing a transputer plus SRAM or DRAM, with the inter-module communications based on the very effective transputer links.

Transtech has a large and expanding range of TRAMs, a sample of which includes:

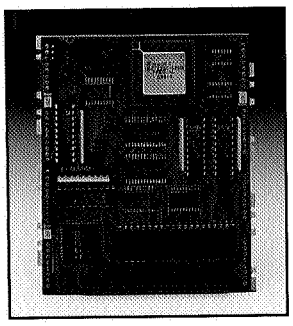
32Bit processoring modules, with an optional on chip floating point unit, and memory from 32KBytes SRAM to 16MBytes of DRAM.

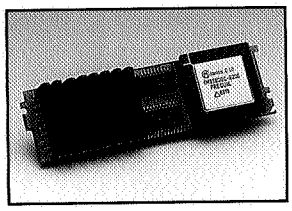
High performance processing modules featuring the IMST801 with a fast non-multiplexed memory interface to between 256K and, currently, 8MBytes of RAM.

Application specific modules with supporting software for a range of graphics TRAMs supporting 512 x 512 8Bit pixels to 1280 x 1024 8Bit pixels, fast on-line disk storage, D to A conversion and EPROM bootable devices.

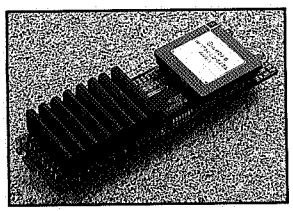
Standard interface modules to communicate with the outside world using RS232, IEEE, Centronics, Ethernet or SCSI.

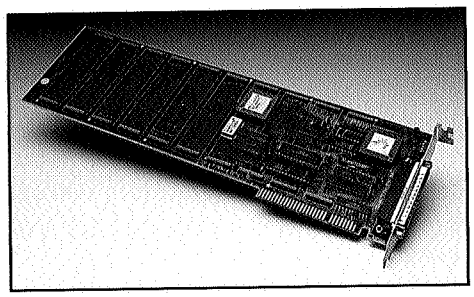
This names but a few, Transtech is currently adding one TRAM per week to its existing range.

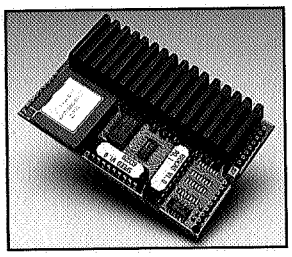


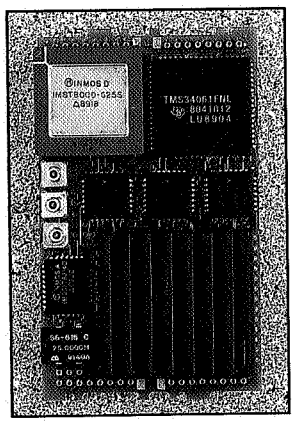


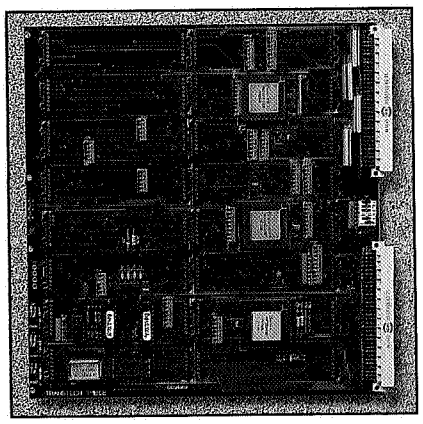
Motherboards are available for a wide range of hosts, these including :- PCAT, PS/2, SUN, HP, APOLLO, MACINTOSH, ATARI ATW, VME and EUROCARD

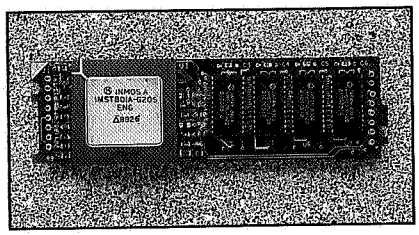








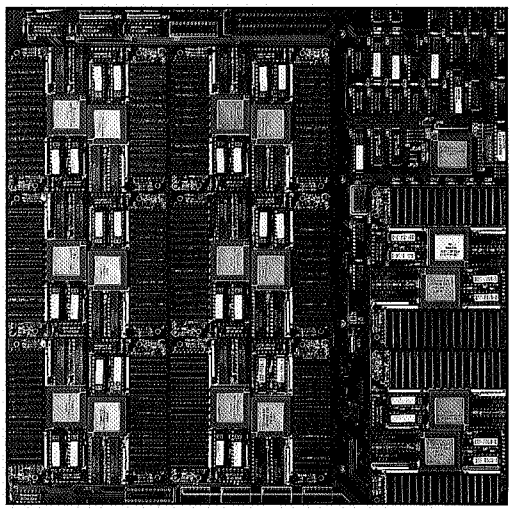




MULTI-COMPUTING PLATFORM

Taking the TRAM range and designing them into the Sun workstation, via a versatile motherboard , has resulted in the evolving family of Multi-Computing Platforms. These offer unrivalled price performance capabilities, based on a modular parallel processing system capable of up to 2.25 MFLOPS per node operating within the Sun environment.

A system in excess of 480 MIPS or 72 MFLOPS is possible from one platform, and with a chassis holding up to 12 platforms the result is staggering amounts of compute power. This operates under the standard UNIX system while running the compilers and library routines available for parallel processing.

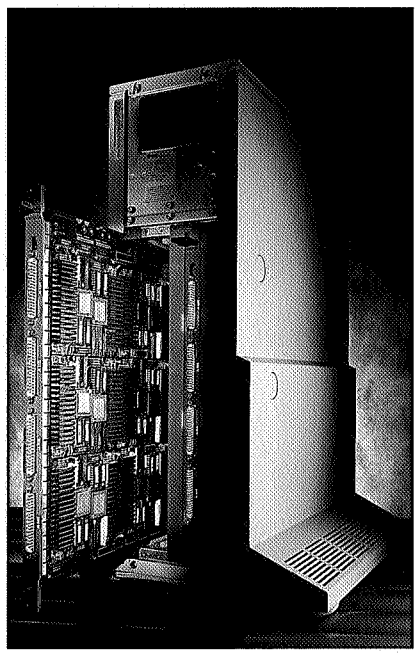


GENESYS

GENESYS is a GENEric operating SYStem which has been designed specifically to meet the requirments of distributed memory, multiple processor systems. Initially implemented on the transputer, GENESYS provides the applications programmer with a flexible but consistent interface to UNIX which allows for maximum utilisation of existing software.

GENESYS is both host and processor independent, and as such embraces the concepts of Open Systems. Transtech is establishing a world-wide collaborative programme to ensure that GENESYS is enhanced and integrated in line with the needs of open systems and parallel processing.

The most important result of this programme is the simplicity and flexibility of creating turnkey high performance systems capable of many 100s of MFLOPs, yet operating within known environments without forsaking any performance or flexibility.



SOFTWARE SUPPORT AND SYSTEMS

All of the current parallel software, compilers and development systems for parallel processing run on the Transtech equipment. Following its total solution commitment Transtech has developed the necessary system installation modules and TRAM support modules, in addition to GENESYS .

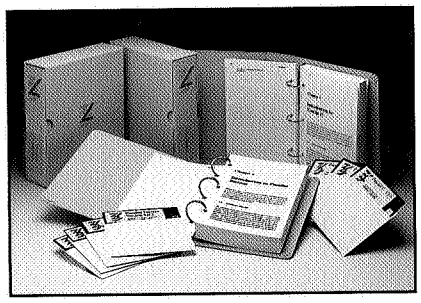
A sample of the software packages available includes:

Standard programming languages such as C, Fortran, Pascal as well as the parallel language occam.

Parallel operating systems for example GENESYS, Trans-Idris, Helios and Express.

Applications packages for X-Windows, disk filing, graphics and engineering analysis.

All relevant new software packages will be supported by Transtech in addition to new products being developed in-house. As future developments come through, Transtech's open system structure will ensure that new software packages will run, where the standards have been adhered to.



FULLY CONFIGURED SYSTEMS

The ease of combination of the Transtech range of products, combined with direct supply agreements with the key hardware suppliers gives Transtech all the elements to supply configured systems.

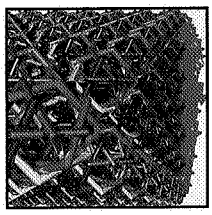
This is further supported by the Transtech open system philosophy, where industry standards are the basis for expansion and evolution, conforming to bus structures, interfaces and data transmission protocols. Future compatibility is ensured via this discipline and it is the only way for the systems designer to avoid the impossible upgrade trap, not least of which is the associated expense. The capability of combining the elements of their product range and to configure the necessary hardware and software in the correct host for the application give Transtech an unrivalled ability to supply solutions, for today and for the future.

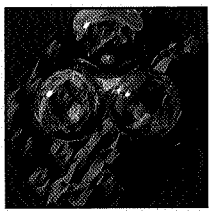
With its combination of expertise, support and experience Transtech is the best choice for the supply of fully configured turnkey solutions to parallel processing needs.

APPLICATIONS

Transtech has delivered over 900 systems and the applications range from financial modelling to real time image processing. Parallel processing has gained recognition world wide as the answer to compute intensive, variable power and distributed processing needs; it is in production equipment for military, space and commercial uses. It is being applied in all areas of computing and by the largest electronics and computer corporations in the world, with particular success in the USA and the Far East.

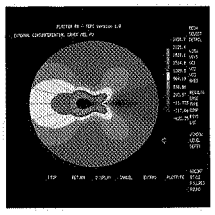
Further examples of Transtech's influence in leading this technology are:-





CENTRAL ELECTRICITY GENERATING BOARD

Engineering analysis plays a vital role in the Nuclear Industry particularly to resolve the questions posed by the Installations Inspectorate. Transputer based PC add-in boards have allowed dedicated and powerful computing resources to be allocated to individual engineers. For instance the multi-tasking of parametric surveys is run at twice the speed as with a VAX 11/780.

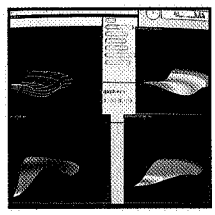


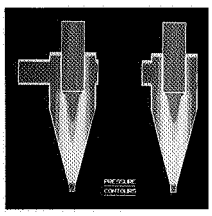
DIGITAL COMMUNICATION SWITCH, CAMBRIDGE CONSULTANTS

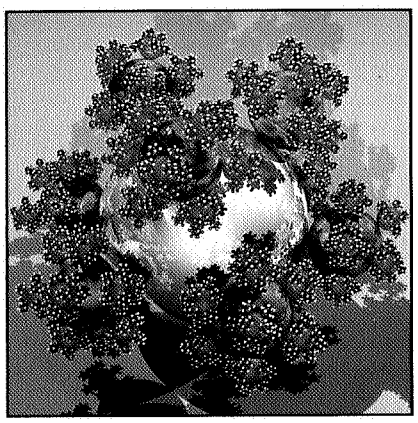
The system is a high density local area network supporting several hundred users and includes a design tolerant to all single fault conditions. Involving 20 man years of effort the project utilises the GENESYS run-time environment to provide communications between software processes on the Sun host and embedded transputer hardware.

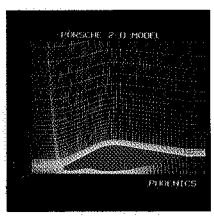
FINITE ELEMENT ANALYSIS, ROCKFIELD SOFTWARE

The applications packages include stress and shock modelling, and simulation of dynamic, transient and fluid systems. Transtech's boards provide the powerful and cost effective, desk top, parallel processing facility.







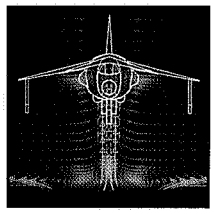


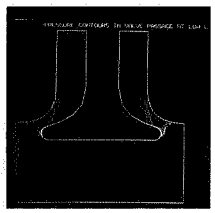
Transtech wishes to extend its thanks to the following companies for their help and contribution to this brochure :-

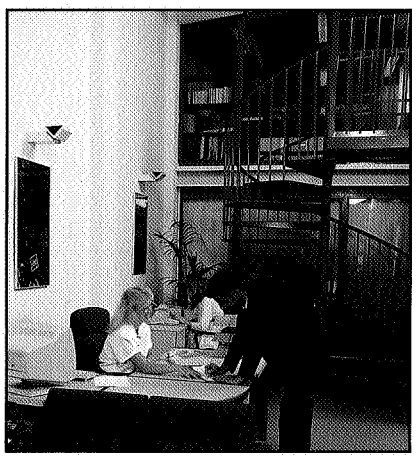
University of Bristol Department of Computer Science, C.H.A.M., National Power Berkeley Nuclear Laboratories, Rockfield Software.

CORNELL THEORY CENTRE, CORNELL UNIVERSITY

The centre, along with the Ohio State Supercomputer Centre, developed the transputer based operating system, Trollius, which forms an integral part of GENESYS. Both universities use the MCP1000 as their main development environment. Transtech is working with both teams to enhance Trollius for other 32-bit processors.







TRANSTECH CUSTOMER LIST

A.E.R.E.

A.R.E.

BBC

BP

BRITISH AEROSPACE

BRITISH TELECOM

B.T.R.L.

C.E.G.B.

C.E.R.N.

CIVIL AVIATION AUTHORITY

COMPUTING DEVICES

DOWTY MARINE

FERRANTI

G.C.H.Q.

G.E.C.

GENERAL ELECTRIC

HEWLETT PACKARD

IBA

IBM

INMOS

I.T.E.C.

MARCONI

MATSUSHITA

MEDICAL RESEARCH COUNCIL

M.E.L.

M.O.D.

MULLARD

N.E.L.

OLIVETTI

PERKIN ELMER

PHILIPS

PLESSEY

R.A.R.D.E.

ROLLS ROYCE

ROYAL AIRCRAFT ESTABLISHMENT

R.S.R.E.

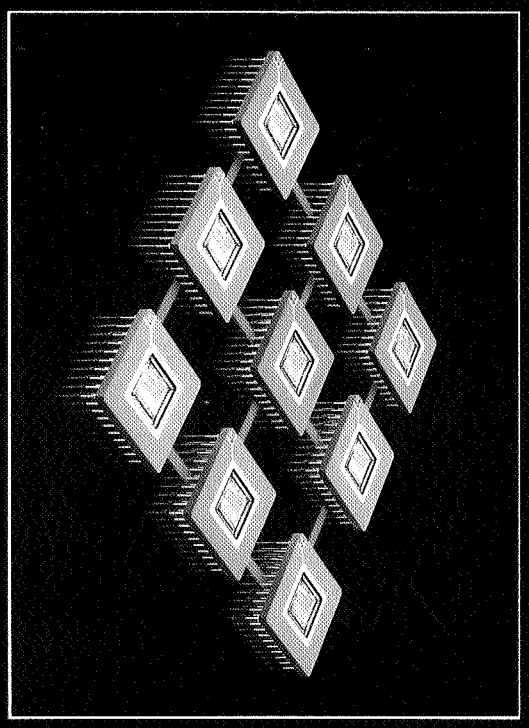
RUTHERFORD LABS

SMITHS INDUSTRIES

TATA ELECTRIC

THORN EMI

UKAEA



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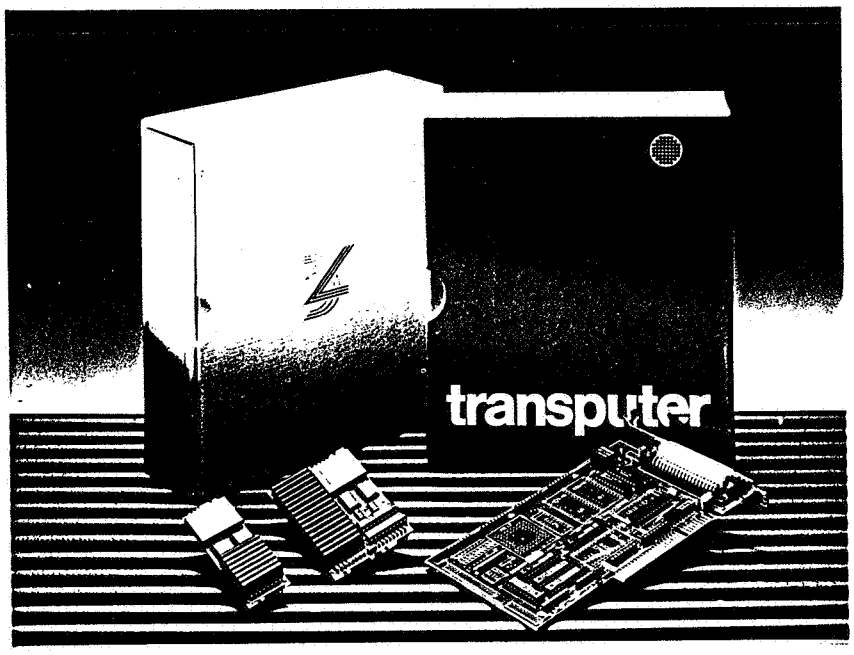
Document Reference: TDLBR1089

TRANSTECH
TRANSPUTER EDUCATIONAL KIT
ED-KIT 1

- **Transtech TMB03 four TRAM slot motherboard for PC AT/XT Bus**
- **TTM6-8-F with IMST800-20 and 2 MBytes zero wait state DRAM**
- **TTM3-8-F with IMST800-20 and 2 MBytes zero wait state DRAM**



Transtech have their Transputer Educational Kit on offer incorporating the new TMB03 low cost TRAM motherboard. The TMB03 can accomodate up to four TRAMs, with up to 10 links available on a standard D-type edge connector. Also provided with the Transputer Educational Kit are two of Transtech's range of TRAMs. The TTM6-8-F has an IMST800 running at 20 MHz with 2 MBytes of fast zero wait state DRAM, while the TTM3-8-F has an IMST800-20 with 1 MByte of fast zero wait state DRAM.

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£1,495.00 ex.vat

with the following software packages available at £500.00 each:
Full Occam TDS
Occam Toolset
3L C, FORTRAN or Pascal

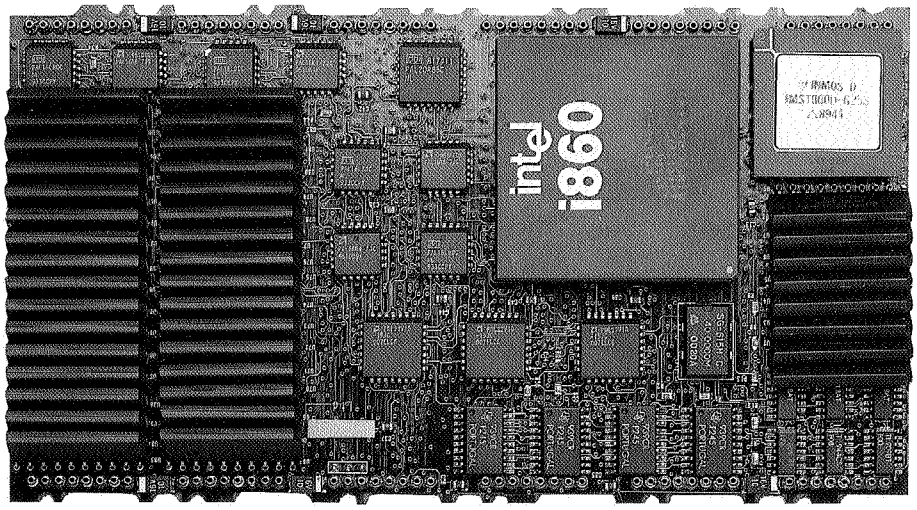
TTM

TRANSTECH TTM100

TTM

Intel i860 TRAM

- Intel i860 40MHz 64-bit Microprocessor
- IMST805 floating point transputer
- 5 to 20 MBytes of fast DRAM
- Sub-system control of reset, analyse and error
- Communicates via 4 transputer serial links
- Industry standard size 6 TRAM format
- Software drivers and maths library support



Introduction The Transtech TTM100 consists of an INTEL i860 64-bit microprocessor, an IMST805 floating point transputer, and 5 to 20 MBytes of fast DRAM. The T805 is configured with 1 or 4 MBytes of local memory, and shares the other 4 or 16 MBytes with the i860.

i860 interface The interface between the i860 and the shared memory system has been optimised to give the i860 zero wait state access for page coherent memory cycles, such as cache fill and cache flush operations. This is achieved using pipeline addressing and page mode access to the DRAM. The i860 busLock function is supported for operating system and other special non-divisible memory cycles.

The inclusion of local RAM for the transputer allows both the i860 and transputer to operate concurrently. A busLock mechanism is included in the transputer shared memory interface to optimise block move operations between local and shared memory.

Synchronisation of the transputer and i860 is achieved by a dual event mechanism. This allows either processor to interrupt the other, invoking specific routines defined in commands passed via areas of shared memory set aside as command control blocks. In this way, either processor can assume the role of system master.

Performance The TTM100 returns the performance of up to 24 30 MHz IMST805's, using the i860 which is capable of 80 MFLOPS (peak single precision), 60 MFLOPS (peak double precision) and 85K Dhrystones.

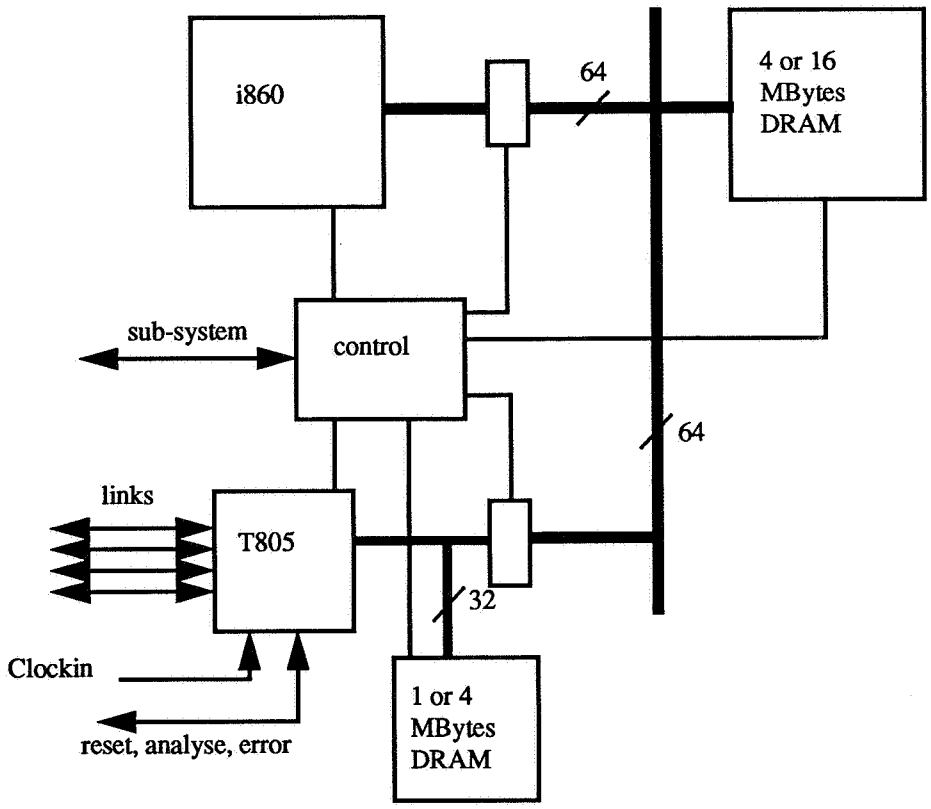
Software The TTM100 is supplied with drivers for use with the Occam TDS, Toolset and 3L compilers, together with an array of over 200 vector library routines optimised to take full advantage of the power of the i860.

TTM

TRANSTECH TTM100

TTM

Intel i860 TRAM



Ordering Information

PART NUMBER	DESCRIPTION
TTM100-4/1	i860 with 4MBytes and T805 with 1Mbyte
TTM100-4/4	i860 with 4MBytes and T805 with 4MBytes
TTM100-16/1	i860 with 16MBytes and T805 with 1MByte
TTM100-16/4	i860 with 16MBytes and T805 with 4MBytes

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DOCUMENT REFERENCE:TTM100FLY0490

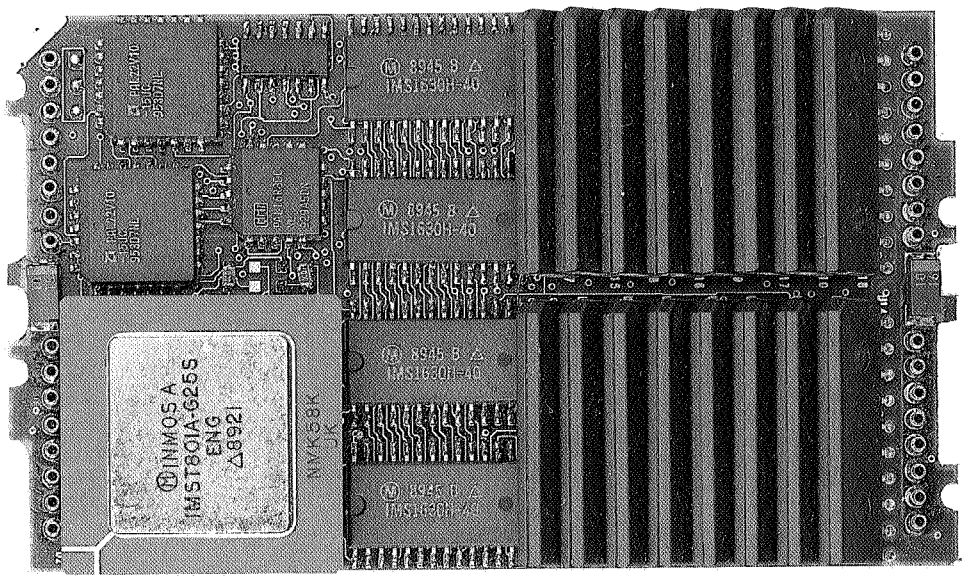
TTM

TRANSTECH TTM32

TTM

High Performance T801 TRAM

- IMST801 floating point transputer
- 2 MBytes of fast 2 cycle page mode DRAM
- 32 KBytes of 2 cycle SRAM
- Sub-system control of reset, analyse and error
- Communicates via 4 transputer serial links
- Industry standard size 2 TRAM format



Introduction The Transtech TTM32 consists of an IMST801 floating point transputer, 2 MBytes of fast 2 cycle page mode DRAM and 32 KBytes of 2 cycle SRAM. It has a sub-system port to control reset, error and analyse.

Memory interface The TTM32 obtains its fast access to the RAM by doing a very quick address comparison on the present DRAM row address and the last DRAM row address, if they are the same the RAM is accessed in two cycles, if they differ the RAM is cycled in the conventional way. This is known as a page break.

The TTM32 also has 32 KBytes of fast SRAM, placed just above internal RAM, which does not cause page breaks when accessed. This allows two areas of very fast external RAM to be available at all times, one of which moves through store with the last DRAM address.

TRANSTECH TTM32

High Performance T801 TRAM

The refresh generator works in burst mode, doing 8 refreshes sequentially so that refreshing, which causes page breaks, has less effect on fast page accesses

The TTM32's fast page is done on 9 bit address boundaries so a page of 512 32-bit words or 2 KBytes of 2 cycle RAM can be accessed in store at any one time.

Having a conventional sub-system port the TTM32 can control a sub-system of other processors, enabling it to run the Occam TDS as a master processor.

TRAM Standard

Measuring only 2.10" by 3.66" (5.33cm by 9.30cm) the TTM32 conforms to the published TRAM standard, allowing them to be plugged easily onto a wide range of motherboards for many different host machines. Up to 10 TRAMs can be accommodated on a Transtech TMB08 board for IBM PC XT or AT's and compatibles, 4 on the Transtech TMB03, TMB04 and TMB05, 16 on a TMB12 double extended eurocard and 32 on the MCP1000 Multi Computing Platform for Sun workstations, allowing rapid prototyping of transputer systems. Transtech TRAMs are also compatible with motherboards from other manufacturers. Further details on the TRAM standard and TRAM Module Motherboard Architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

Ordering Information

PART NUMBER	DESCRIPTION
TTM32-25	IMST801-25 transputer with 32 KBytes SRAM and 2 MBytes DRAM
TTM32-30	IMST801-30 transputer with 32 KBytes SRAM and 2 MBytes DRAM

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DOCUMENT REFERENCE:TTM32FLY0390

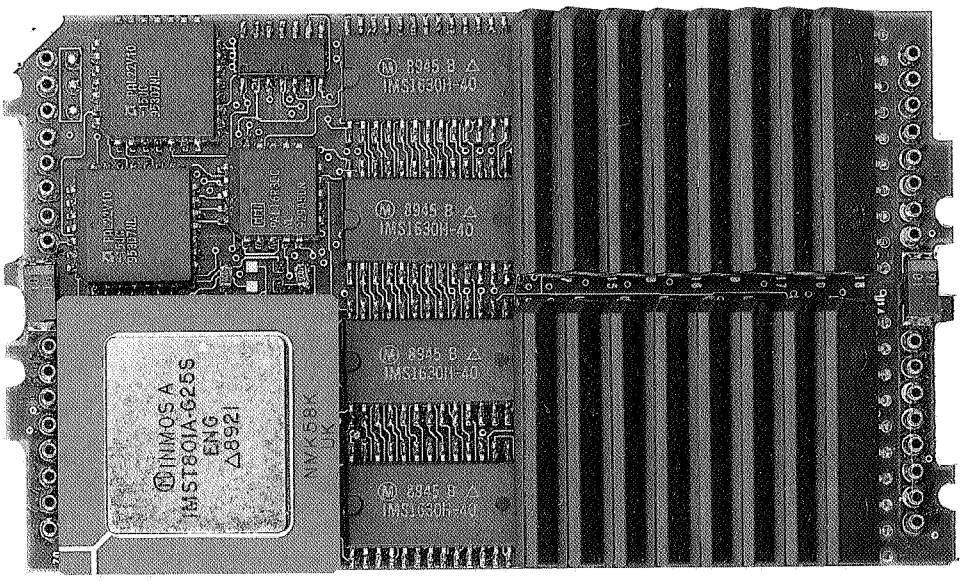
TTM

TRANSTECH TTM34

TTM

High Performance T801 TRAM

- IMST801 floating point transputer
- 4 MBytes of fast 2 cycle page mode DRAM
- 32 KBytes of 2 cycle SRAM
- Sub-system control of reset, analyse and error
- Communicates via 4 transputer serial links
- Industry standard size 2 TRAM format



Introduction The Transtech TTM34 consists of an IMST801 floating point transputer, 4 MBytes of fast 2 cycle page mode DRAM and 32 KBytes of 2 cycle SRAM. It has a sub-system port to control reset, error and analyse.

Memory interface The TTM34 obtains its fast access to the RAM by doing a very quick address comparison on the present DRAM row address and the last DRAM row address, if they are the same the RAM is accessed in two cycles, if they differ the RAM is cycled in the conventional way. This is known as a page break.

The TTM34 also has 32 KBytes of fast SRAM, placed just above internal RAM, which does not cause page breaks when accessed. This allows two areas of very fast external RAM to be available at all times, one of which moves through store with the last DRAM address.

TTM

TRANSTECH TTM34

TTM

High Performance T801 TRAM

The refresh generator works in burst mode, doing 8 refreshes sequentially so that refreshing, which causes page breaks, has less effect on fast page accesses

The TTM34's fast page is done on 9 bit address boundaries so a page of 512 32-bit words or 2 KBytes of 2 cycle RAM can be accessed in store at any one time.

Having a conventional sub-system port the TTM34 can control a sub-system of other processors, enabling it to run the Occam TDS as a master processor.

TRAM Standard

Measuring only 2.10" by 3.66" (5.33cm by 9.30cm) the TTM34 conforms to the published TRAM standard, allowing them to be plugged easily onto a wide range of motherboards for many different host machines. Up to 10 TRAMs can be accommodated on a Transtech TMB08 board for IBM PC XT or AT's and compatibles, 4 on the Transtech TMB03, TMB04 and TMB05, 16 on a TMB12 double extended eurocard and 32 on the MCP1000 Multi Computing Platform for Sun workstations, allowing rapid prototyping of transputer systems. Transtech TRAMs are also compatible with motherboards from other manufacturers. Further details on the TRAM standard and TRAM Module Motherboard Architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

Ordering Information

PART NUMBER	DESCRIPTION
TTM34-25	IMST801-25 transputer with 32 KBytes SRAM and 4 MBytes DRAM
TTM34-30	IMST801-30 transputer with 32 KBytes SRAM and 4 MBytes DRAM

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DOCUMENT REFERENCE:TTM34FLY0390

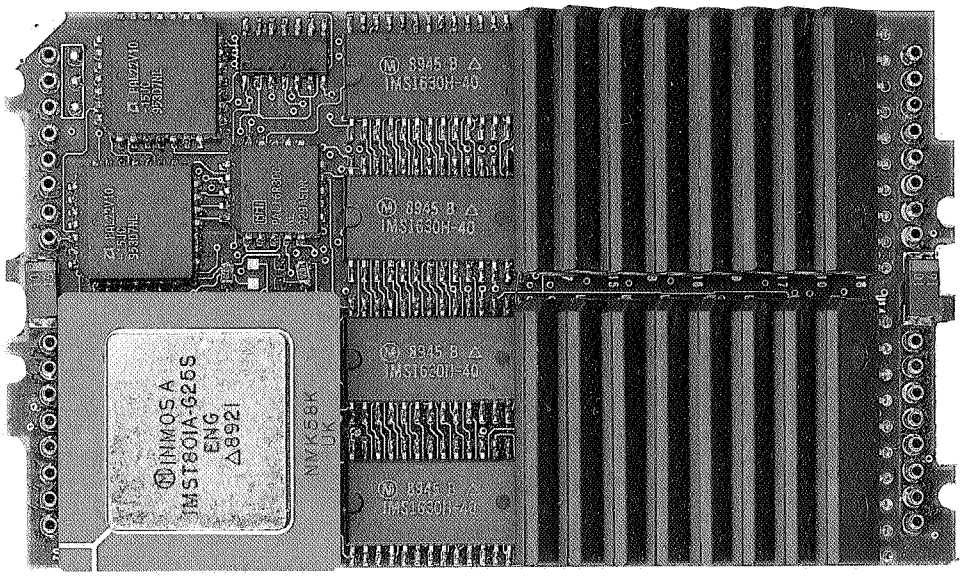
TTM

TRANSTECH TTM38

TTM

High Performance T801 TRAM

- IMST801 floating point transputer
- 8 MBytes of fast 2 cycle page mode DRAM
- 32 KBytes of 2 cycle SRAM
- Sub-system control of reset, analyse and error
- Communicates via 4 transputer serial links
- Industry standard size 2 TRAM format



Introduction The Transtech TTM38 consists of an IMST801 floating point transputer, 8 MBytes of fast 2 cycle page mode DRAM and 32 KBytes of 2 cycle SRAM. It has a sub-system port to control reset, error and analyse.

Memory interface The TTM38 obtains its fast access to the RAM by doing a very quick address comparison on the present DRAM row address and the last DRAM row address, if they are the same the RAM is accessed in two cycles, if they differ the RAM is cycled in the conventional way. This is known as a page break.

The TTM38 also has 32 KBytes of fast SRAM, placed just above internal RAM, which does not cause page breaks when accessed. This allows two areas of very fast external RAM to be available at all times, one of which moves through store with the last DRAM address.

TTM

TRANSTECH TTM38

TTM

High Performance T801 TRAM

The refresh generator works in burst mode, doing 8 refreshes sequentially so that refreshing, which causes page breaks, has less effect on fast page accesses

The TTM38's fast page is done on 9 bit address boundaries so a page of 512 32-bit words or 2 KBytes of 2 cycle RAM can be accessed in store at any one time.

Having a conventional sub-system port the TTM38 can control a sub-system of other processors, enabling it to run the Occam TDS as a master processor.

TRAM Standard

Measuring only 2.10" by 3.66" (5.33cm by 9.30cm) the TTM38 conforms to the published TRAM standard, allowing them to be plugged easily onto a wide range of motherboards for many different host machines. Up to 10 TRAMs can be accommodated on a Transtech TMB08 board for IBM PC XT or AT's and compatibles, 4 on the Transtech TMB03, TMB04 and TMB05, 16 on a TMB12 double extended eurocard and 32 on the MCP1000 Multi Computing Platform for Sun workstations, allowing rapid prototyping of transputer systems. Transtech TRAMs are also compatible with motherboards from other manufacturers. Further details on the TRAM standard and TRAM Module Motherboard Architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

Ordering Information

PART NUMBER	DESCRIPTION
TTM38-25	IMST801-25 transputer with 32 KBytes SRAM and 8 MBytes DRAM
TTM38-30	IMST801-30 transputer with 32 KBytes SRAM and 8 MBytes DRAM

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DOCUMENT REFERENCE:TTM38FLY0390

TMB

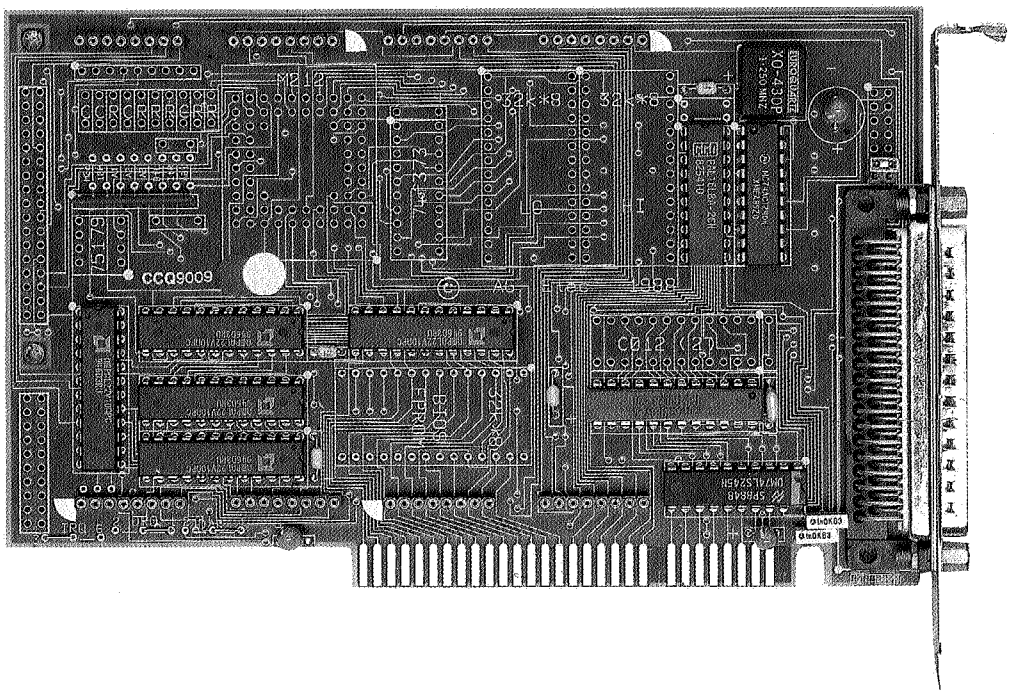
Transtech TMB03

TMB

A TRANSPUTER MODULE MOTHERBOARD FOR THE IBM PC

Features

- **Four TRAM (TRAnsputer Module) slots**
- **Plugs directly into IBM PC AT or XT and compatibles**
- **DMA/IRQ capability for fast MS.DOS I/O transfer**
- **Supports Occam TDS development and 3L's scientific languages**
- **Compatible with the Transtech range of TRAMs**



Introduction The TMB03 is a low cost 4 TRAM motherboard for IBM PC XT and AT compatible machines. Ten of the links are hardwired to the D-type edge connector, allowing networks with external connections to be configured.

IBM PC Bus Interface An interface to the PC bus is provided via an IMSC012 link adaptor for communication between the host machine and a transputer network. The interface supports software polling of the link adaptor, used in many earlier transputer boards and also a DMA mechanism allowing transfer rates of between 200 and 300 KBytes/sec to be achieved. The TMB03 also has the ability to interrupt the host PC on a number of user defined events.

Transtech TMB03

System Control The reset, error and analyse system control of the TRAMs is user definable, by selecting one of a variety of reset configurations. TRAM slot 0 can be reset either from the exeternal world via the edge connector, or from the PC, while the remaining TRAM slots 1 to 9 can be reset either from the same source as TRAM 0 or from a subsystem generated by TRAM 0

Compatibility The TMB03 accepts the whole range of TRAMs from Transtech and is compatible with those of other manufacturers, giving customers the freedom to choose many different processor and memory combinations or application specific TRAMs. Information on the range of Transtech TRAMs is available from Transtech or your local distributor. Further details on the TRAM standard and TRAM motherboard architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

Software The TMB03 can be programmed with software development packages to run Occam, C, FORTRAN, Pascal and other transputer language compilers as well as Helios, TransIDRIS, Express and other transputer operating systems. It can also be used as the processing hardware for a number of application specific software packages that are available for the transputer.

Ordering Information

PART NUMBER	DESCRIPTION
TMB03	IBM PC FORMAT TRAM MOTHERBOARD WITH 4 TRAM SLOTS

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DOCUMENT REFERENCE:TMB03FLY0390

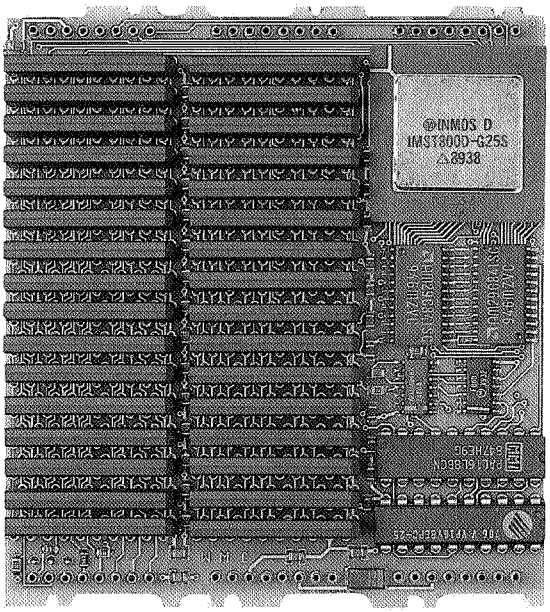
TTM

Transtech TTM19
Sixteen MByte TRAM

TTM

Features

- **IMST800, IMST425 or IMST414 transputer options**
- **16 MBytes of dynamic RAM**
- **Zero wait state memory option**
- **20, 25 or 30 MHz transputer speed option**
- **Four serial transputer links**
- **Only 16 active pins**
- **Industry standard size 3 TRAM**
- **Compatible with Transtech range of TRAM motherboards**
- **Full Sub-system control**



Introduction The Transtech TTM19 TRAM (TRAnsputer Module) is a small industry standard daughterboard for the Transtech range of TRAM motherboards. It has 16 MBytes of dynamic RAM and is capable of supporting the IMST800, IMST425 and IMST414 transputers. It also has the ability to control a sub-system of transputers.

TRAM Standard Measuring only 3.15" by 3.66" (8.00cm by 9.30cm) the TTM19 conforms to the published TRAM standard, allowing them to be plugged easily onto a wide range of motherboards for many different host machines. Up to 10 TRAMs can be accommodated on a Transtech TMB08 board for IBM PC XT or AT's and compatibles, 4 on the Transtech TMB04 and TMB05, 16 on a TMB12 double extended eurocard and 32 on the MCP1000 Multi Computing Platform, allowing rapid prototyping of transputer systems. Transtech TRAMs are also compatible with motherboards from other manufacturers. Further details on the TRAM standard and TRAM Module Motherboard Architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

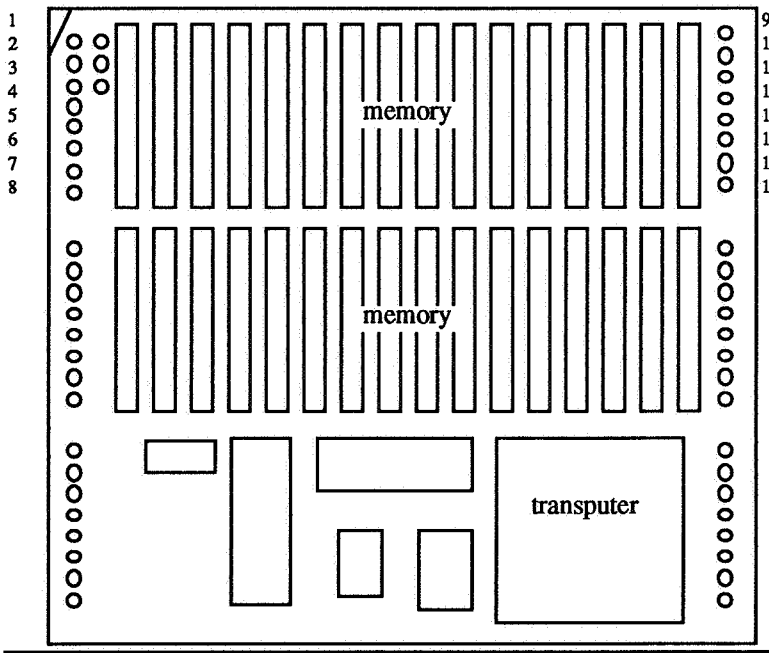
TTM

Transtech TTM19

TTM

Functional Description

TRAMs use 16 pins for communication with the motherboard and for obtaining power. However, TRAMs that are larger than size 1 have more than 16 pins, with the extra pins providing more power and ground connections. The extra pins also propagate the signals from the motherboard below to allow stacking of modules. The link speed of the TRAMs is selected by two pins. When both are held low the links operate at 10 Mbits/sec and when high at 20 Mbits/sec. This is implemented by jumpers or switches on the motherboards. The allocation of the pins are shown in the following diagram.



1 Link2Out
2 Link2In
3 VCC
4 Link1Out
5 Link1In
6 LinkSpeedA
7 LinkSpeedB
8 ClockIn(5MHz)
9 Link3In
10 Link3Out
11 GND
12 Link0In
13 Link0Out
14 notError
15 Reset
16 Analyse

Ordering Information

Part Number	Processor Type	Processor Cycle Time (ns)	Memory (MBytes)	Memory CycleTime (ns)
TTM19-4-F	IMST414-20	50	16	150
TTM19-42-F	IMST425-20	50	16	150
TTM19-8-F	IMST800-20	50	16	150
TTM19-85	IMST800-25	40	16	160
TTM19-85-F	IMST800-25	40	16	120
TTM19-830	IMST800-30	33	16	132

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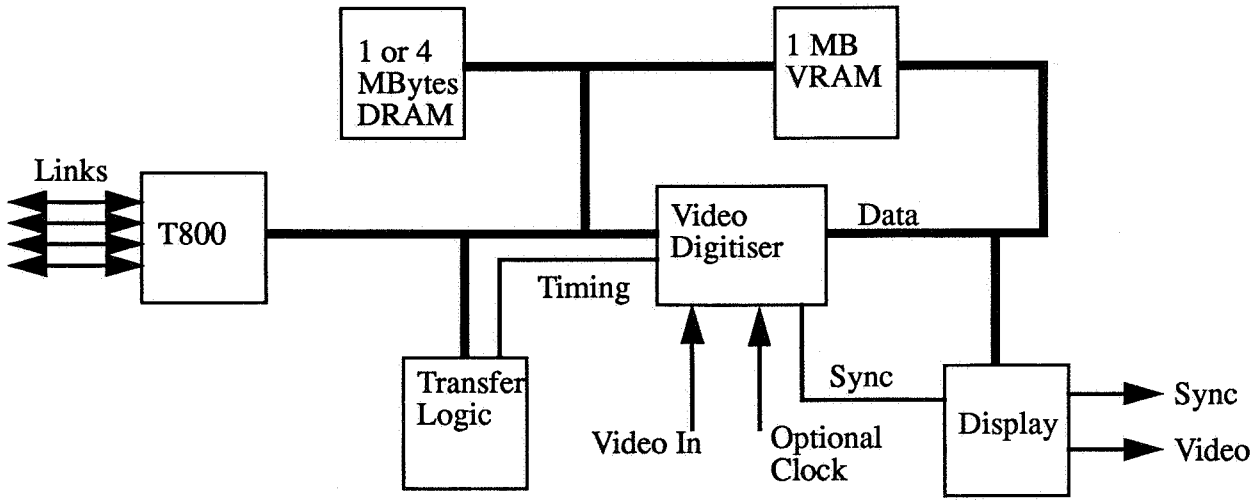
DOCUMENT REFERENCE:TTM19FLY0390

TRANSTECH TTG-F

Video Framegrabber TRAM

- **IMST800 floating point transputer**
- **1 or 4 MBytes of fast DRAM**
- **1 MByte VRAM**
- **Real time image capture**
- **Supports up to 1024 x 1024 8-bit pixels**
- **Sub-system control of reset, analyse and error**
- **Communicates via 4 transputer serial links**
- **Industry standard size 4 TRAM format**



Introduction The Transtech TTG-F consists of an IMST800, running at 25MHz, floating point transputer, 1 or 4 MBytes of fast DRAM and 1 MByte of VRAM. It also has a Brooktree BT251 video digitiser and an IMSG178 colour palette chip.

Video Capture The TTG-F is a real time image capturing device for transputer based systems, capable of digitising images of up to 1024 x 1024 8-bit pixels at up to 18 Msps. The 1 MByte of Video RAM can hold up to 4 separate images at any one time (depending on image size). Three video inputs are software switchable as well as the resolution being software selectable. The transfer logic can capture single frames or continuous video. The TTG-F has software support for direct digitisation of PAL and NTSC monochrome video. For capture of RGB 24-bit video three TTG-F's can be synchronised. The TTG-F also has an IMSG178 colour palette chip allowing it to display the live digitised video in the same format as it was captured.

TTG

TRANSTECH TTG-F

TTG

Video Framegrabber TRAM

Image Processing

The TTG-F also has an IMST800 plus 1 or 4 MBytes of DRAM for program use, which allows image processing tasks to be carried out on the TTG-F without the images having to be transferred to other processing modules. However if images need to be transferred all four transputer links are available, enabling real time video at approx 600 x 400 8-bit pixels to be transferred. Coupled with the Transtech TTG1 or TTG3 graphics TRAM's the TTG-F provides a highly flexible image capture, processing and display system.

Software

The TTG-F is supplied with software drivers for programming the options of sampling rate, display resolution and video input as well as an image processing library callable from the Occam TDS, Occam Toolset or the 3L scientific language compilers.

TRAM Standard

Measuring only 4.20" by 3.66" (10.66cm by 9.30cm) the TTG-F conforms to the published TRAM standard, allowing them to be plugged easily onto a wide range of motherboards for many different host machines. Up to 10 TRAMs can be accommodated on a Transtech TMB08 board for IBM PC XT or AT's and compatibles, 4 on the Transtech TMB03, TMB04 and TMB05, 16 on a TMB12 double extended eurocard and 32 on the MCP1000 Multi Computing Platform for Sun workstations, allowing rapid prototyping of transputer systems.

Ordering Information

PART NUMBER	DESCRIPTION
TTG-F1	Framegrabber with IMST800 and 1 MByte DRAM
TTG-F4	Framegrabber with IMST800 and 4 MBytes DRAM

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DOCUMENT REFERENCE:TTG-FFLY0390

TMB

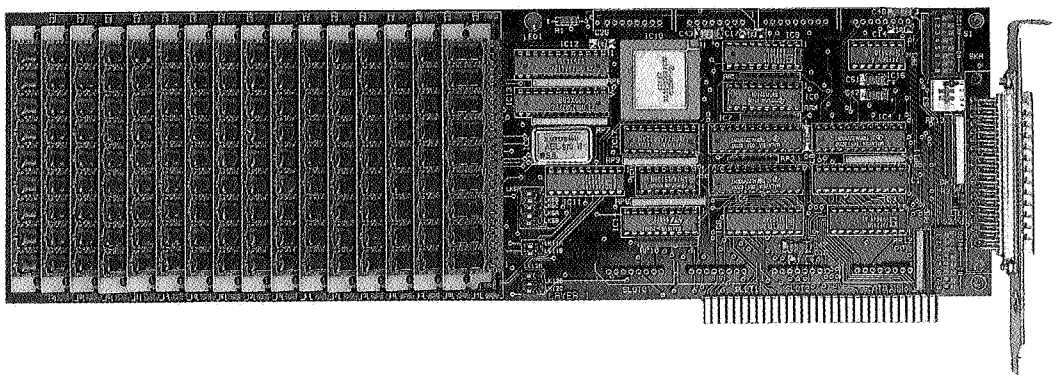
Transtech TMB04

TMB

AN EXPANDABLE TRANSPUTER BOARD FOR THE IBM PC

Features

- **IMST800, IMST425 or IMST414 transputer options**
- **1 to 16 MBytes of dynamic RAM with zero wait state option**
- **20, 25 or 30 MHz transputer speed options**
- **Four standard TRAM slots**
- **DMA/IRQ capability for fast MS.DOS I/O transfer**
- **Plugs directly into IBM PC AT or XT and compatibles**
- **Supports Occam TDS development and 3L's scientific languages**
- **Compatible with the Transtech range of TRAMs**



Introduction The Transtech TMB04 is part of a compatible family of transputer development boards. The TMB04 will fit any IBM PC AT or XT (and compatibles) expansion slot, providing the interface between the PC running a file server under MS.DOS and the processing power of transputer systems.

Flexibility The TMB04 has been developed with Transtech's unrivalled experience of transputer boards to provide the most flexible single transputer board available.

Capable of supporting any speed variant of the IMST800, IMST425 and IMST414 transputers, the TMB04 also has options for 1,2,4,8 or 16 MBytes of DRAM, which can be accessed in 3,4,5 or 6 cycles depending on the speed of processor and memory. The four links of the transputer can be accessed via a standard 37-way D-type edge connector compatible with a wide range of other transputer boards. These links can be set to run at 10 or 20 Mbits/sec.

Transtech TMB04

IBM PC Bus Interface An interface to the PC bus is provided via an IMSC012 link adaptor for communication between the host machine and a transputer network. The interface supports software polling of the link adaptor, used in many earlier transputer boards and also a DMA mechanism allowing transfer rates of between 200 and 300 KBytes/sec to be achieved. The TMB04 also has the ability to interrupt the host PC on a number of user defined events.

Expandable More flexiblity is provided by the addition of four TRAM (TRAnsputer Module) slots, which allow up to four standard TRAMs to be added to the board. The TMB04 accepts the whole range of TRAMs from Transtech and is compatible with those of other manufacturers, giving customers the freedom to choose many different processor and memory combinations or application specific TRAMs. Eight links from the four TRAM slots are also taken to the 37-way D-type edge connector, allowing them to be connected to external devices as well as to the master transputer on the TMB04. Further information on the Transtech range of TRAMs is available from Transtech or your local distributor, while details on the TRAM standard and TRAM motherboard architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

System Control The reset, error and analyse system control of the transputer is user definable, by selecting one of a variety of reset configurations. The master transputer can be reset either from the external world via the edge connector, or from the PC, while the remaining TRAM slots can be reset from either the same source as the master transputer or from a sub-system generated by the TMB04. The generation of the sub-system enables the TMB04 to control a large system of transputers while still running the TDS.

Software The TMB04 can be programmed with software development packages to run Occam, C, FORTRAN, Pascal and other transputer language compilers as well as the Helios, TransIDRIS, Express and other transputer operating systems. It can also be used as the processing hardware for a number of application specific software packages that are available for the transputer. The board is also supplied with a diagnostic test program.

Ordering Information

TMB04 -	PROCESSOR OPTION	MEMORY OPTION
	A=IMST414-20 B=IMST425-20 C=IMST425-25 D=IMST425-30 E=IMST800-20 F=IMST800-25 G=IMST800-30	1=1 MBYTE 2=2 MBYTES 4=4 MBYTES 8=8 MBYTES 16=16 MBYTES

FAST 3 CYCLE RAM IS AVAILABLE FOR ALL 20 MHz PROCESSOR OPTIONS AND SHOULD BE SPECIFIED BY ADDING "F" TO THE PART NUMBER e.g.TMB04-E-2F HAS AN IMST800-20 WITH 2 MBYTES OF FAST 3 CYCLE DRAM

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Document Reference:TMB04FLY0789

TMB

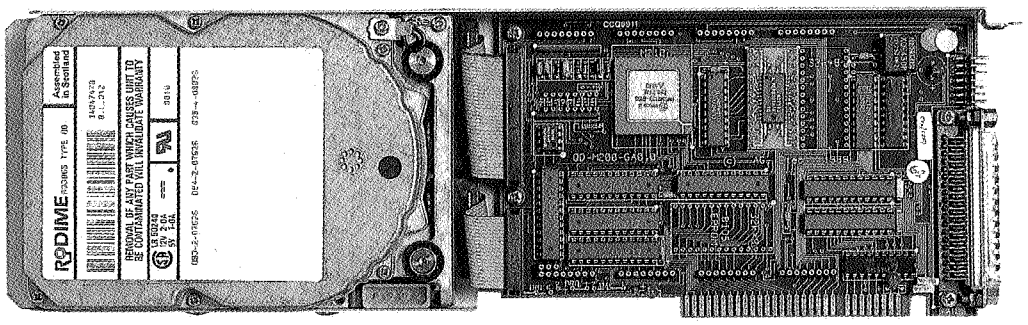
Transtech TMB05

TMB

A TRANSPUTER SYSTEM HARD DISK BOARD

Features

- **IMSM212 transputer disk controller**
- **20 or 55 MByte fast (28 ms) winchester disk drive**
- **Plugs directly into IBM PC AT or XT and compatibles**
- **Four TRAM slots**
- **Enhances execution speed of transputer systems**
- **DMA/IRQ capability for fast MS.DOS I/O transfer**
- **TDOS/TBIOS software support for Occam TDS and 3L scientific languages**
- **Compatible with Transtech range of TRAMs**



Introduction The Transtech TMB05 is an IBM PC AT or XT (and 100% compatibles) expansion board capable of hosting upto four TRAMs (TRAnsputer Modules). It provides an IMSM212 16-bit transputer disk controller to interface both the PC bus and transputer systems to the fast winchester disk drive.

Functional Description The TSB05's disk interface is controlled by the IMSM212 transputer which has one of its two serial links attached to the IBM I/O bus via a link adaptor. A program loaded to the IMSM212 enables it to interpret DOS commands, making the disk the next logical drive in the system, providing an easy method of loading existing software to and from it. The second serial link of the IMSM212 is brought to the standard 37-way D-type edge connector to allow the TMB05 to be connected to an external transputer system or to be reconnected to a TRAM in one of the TRAM slots on the board.

Transtech TMB05

IBM PC Bus Interface An interface to the PC bus is provided via an IMSC012 link adaptor for communication between the host machine and a transputer network. The interface supports software polling of the link adaptor, used in many earlier transputer boards and also a DMA mechanism allowing transfer rates of between 200 and 300 KBytes/sec to be achieved. The TMB05 also has the ability to interrupt the host PC on a number of user defined events.

Expandable More flexibility is provided by the addition of four TRAM (TRAnsputer Module) slots, which allow up to four standard TRAMs to be added to the board. The TMB05 accepts the whole range of TRAMs from Transtech and is compatible with those of other manufacturers, giving customers the freedom to choose many different processor and memory combinations or application specific TRAMs. Ten links from the four TRAM slots are also taken to the 37-way D-type edge connector, allowing them to be connected to external devices. Further information on the Transtech range of TRAMs is available from Transtech or your local distributor, while details on the TRAM standard and TRAM motherboard architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

System Control The reset, error and analyse system control of the transputers is user definable, by selecting one of a variety of reset configurations. The IMSM212 and TRAM slot 0 can be reset either from the external world via the edge connector, or from the PC, while the remaining TRAM slots can be re-set either from the same source or from a subsystem generated on the TRAM in slot 0. The generation of the sub-system enables the TMB05 to control a much larger system of transputers.

Software The TMB05 is supplied with system software that enables it to intercept all file I/O operations before the slow IBM PC bus is involved.

Software developers using Occam, can include the TBIOS (Transputer BIOS) as a library function to provide fast and efficient access to the IMSM212. Alternatively the use of TDOS which comprises the TBIOS routines provides a shell from which to run applications such as the TDS (Transputer Development System). Full listings of Occam examples to interface to the TBIOS are provided.

Users of the 3L scientific languages can run TBIOS as a separate task, and use channel communication from their application to access the mass store directly, without going through layers of unwieldly protocols. Examples are provided in each language to emulate the required primitives open, read, write and close file structured I/O. These primitives are implemented in as near a 'look alike' form as the inherent language primitives to allow simple mass editing of existing code to run under this system.

A RAMDISK utility provided with the TBIOS allows the user to create automatic caching of files to memory without major program changes.

Ordering Information

PART NUMBER	DESCRIPTION
TMB05-20	TRANSPUTER HARD DISK BOARD WITH 20 MBYTE WINCHESTER
TMB05-55	TRANSPUTER HARD DISK BOARD WITH 55 MBYTE WINCHESTER

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Document Reference:TMB05FLY0789

TMB

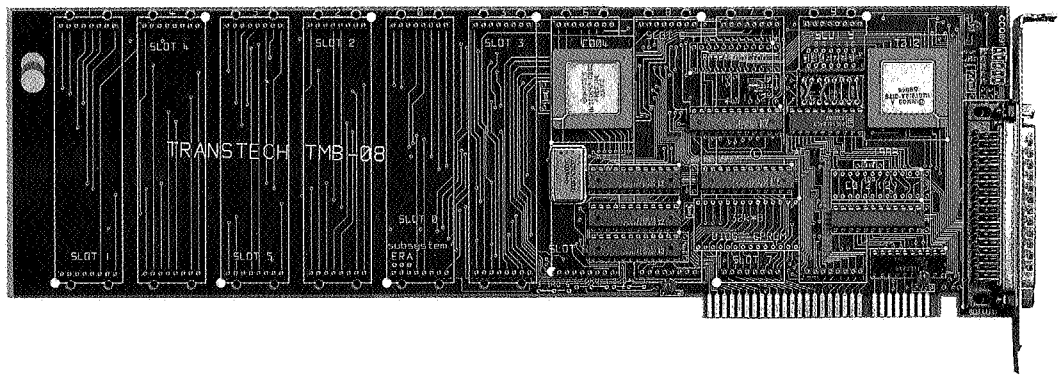
Transtech TMB08

TMB

A TRANSPUTER MODULE MOTHERBOARD FOR THE IBM PC

Features

- **Ten TRAM (TRAnsputer Module) slots**
- **Plugs directly into IBM PC AT or XT and compatibles**
- **Includes IMSC004 link crossbar switch for configurable reconnectivity**
- **Supplied with network configuration software**
- **DMA/IRQ capability for fast MS.DOS I/O transfer**
- **Supports Occam TDS development and 3L's scientific languages**
- **Compatible with the Transtech range of TRAMs**
- **Fully compatible superset of Inmos IMSB008**



Introduction The TMB08 is a 10 TRAM motherboard for IBM PC XT and AT compatible machines. It incorporates a link crossbar switch (IMSC004) allowing user configuration of network topologies. Eight of the links connected to the C004 are hardwired to the D-type edge connector, allowing networks with external connections to be configured.

IBM PC Bus Interface An interface to the PC bus is provided via an IMSC012 link adaptor for communication between the host machine and a transputer network. The interface supports software polling of the link adaptor, used in many earlier transputer boards and also a DMA mechanism allowing transfer rates of between 200 and 300 KBytes/sec to be achieved. The TMB08 also has the ability to interrupt the host PC on a number of user defined events.

TMB

Transtech TMB08

TMB

Software Link Configuration

The ten TRAM slots are connected in a default pipeline using links 1 and 2. The remaining links 0 and 3 from each site are connected to the C004. The user may programme the C004 directly from software, thereby 'softwiring' the links to the desired configuration. This process may be repeated, thus enabling the user to evaluate a variety of network topologies for a given application. The C004 is programmed, in the default configuration, from a T222 16 bit transputer which allows the configuration pipeline to be cascaded for multiple board systems. For a single TMB08 board the C004 can be programmed via a second optional link adaptor from an EXE running on the PC, enabling the link configuration to be set up on power on.

System Control

The reset, error and analyse system control of the TRAMs is user definable, by selecting one of a variety of reset configurations. TRAM slot 0 can be reset either from the exeternal world via the edge connector, or from the PC, while the remaining TRAM slots 1 to 9 can be reset either from the same source as TRAM 0 or from a subsystem generated by TRAM 0

IMSB008 Superset

The TMB08 is a superset of the Inmos IMSB008 with additional options including a site for an EPROM in the PC address map to hold boot code, a second link adaptor for programming the C004, and the capability to reset each individual TRAM slot by control from the T222.

Compatibility

The TMB08 accepts the whole range of TRAMs from Transtech and is compatible with those of other manufacturers, giving customers the freedom to choose many different processor and memory combinations or application specific TRAMs. Information on the range of Transtech TRAMs is available from Transtech or your local distributor. Further details on the TRAM standard and TRAM motherboard architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

Software

The TMB08 can be programmed with software development packages to run Occam, C, FORTRAN, Pascal and other transputer language compilers as well as Helios, TransIDRIS, Express and other transputer operating systems. It can also be used as the processing hardware for a number of application specific software packages that are available for the transputer. The board is also supplied with a diagnostic test program and system software for programming the IMSC004 cross-bar switch.

Ordering Information

PART NUMBER	DESCRIPTION
TMB08	IBM PC FORMAT TRAM MOTHERBOARD WITH 10 TRAM SLOTS

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Document Reference:TMB08FLY0789

TMB

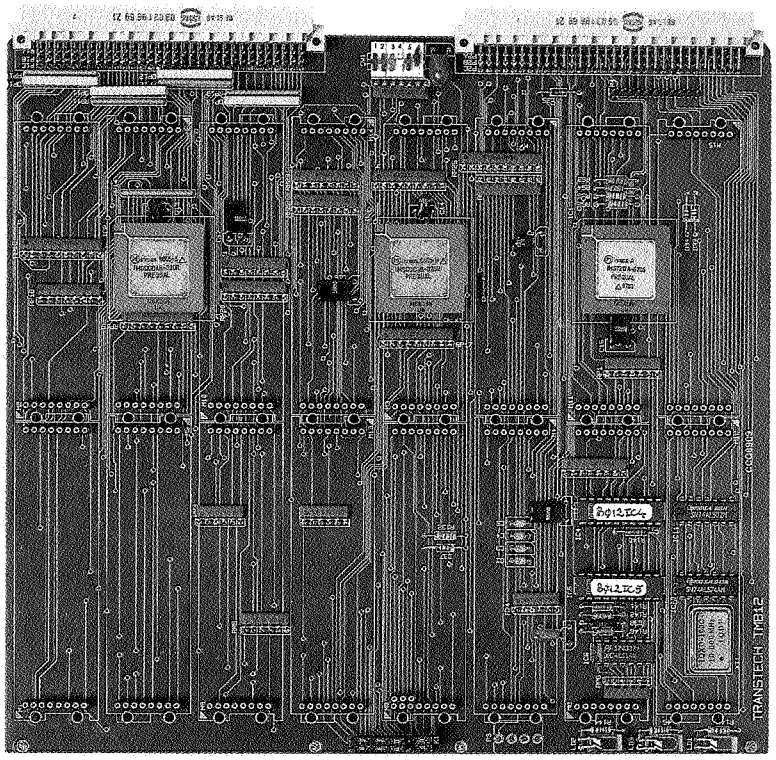
Transtech TMB12

TMB

A DOUBLE EXTENDED EUROCARD TRANSPUTER MODULE MOTHERBOARD

Features

- **Sixteen standard TRAM (TRAnsputer Module) slots**
- **IMST800, IMST425 or IMST414 transputer options**
- **Includes two IMSC004 link crossbar switches**
- **Software reconfigurable link topology**
- **Plugs directly into Transtech TRANSRACK10/12 and Inmos ITEM**
- **Compatible with the Transtech range of TRAMs**



Introduction The Transtech TMB12 is a double extended eurocard with 16 TRAM (TRAnsputer Module) slots. It incorporates 2 IMSC004 link crossbar switches controlled by a 16 bit IMST222 transputer, for software programming of the link topology of the transputer network.

Flexibility Flexibility is provided by the TRAM slots, which allow up to sixteen standard TRAMs to be added to the board. The TMB12 accepts the whole range of TRAMs from Transtech and is compatible with those of other manufacturers, giving customers the freedom to choose many different processor and memory combinations or application specific TRAMs. Further information on the Transtech range of TRAMs is available from Transtech or your local distributor, while details on the TRAM standard and TRAM motherboard architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

Transtech TMB12

Link Configuration

The 16 TRAM slots are arranged in a hardwired pipeline with their links 2 to 1 connected together. The ends of the pipeline are taken to the P2 connector for connection to other transputer boards or external devices.

All the slots link 0 outputs and link 3 inputs are connected to one IMSC004 with the remaining link input and outputs of the IMSC004 connected to the P1 connector. The other IMSC004 is connected similarily to all the link 0 inputs and link 3 outputs from the 16 slots and to the P1 connector.

This connection scheme allows a link 0 from any slot to be connected to a link 3 from any slot but not to another slots link 0. Slot 0 Link 0 is not however directly connected to the IMSC004's but to the P2 connector and can be connected to the IMSC004's by use of a jumper. This allows two links from slot 0 to be connected via P2 to external boards or devices which may be required in some applications where the use of the IMSC004's is not required.

Programming the IMSC004's

The IMSC004's each have a configuration link into which the link configuration information is passed by the IMST222 16 bit transputer. The IMST222 is connected by its link 0 and link 3 to the IMSC004's, while its other links 1 and 2 are taken to the P2 connector and are called 'ConfigUp' and 'ConfigDown' respectively. These two links allow the IMSC004's to be programmed from an external development system and for the TMB12 to pass on configuration information to other boards from the development system. The board is also supplied with a software system for programming the 16-bit IMST222 transputer which in turn programs the two IMSC004 crossbar switches to set up the desired link configurations.

System Control

The reset, error and analyse system control of the transputer is user definable, by selecting one of a variety of reset configurations. Slot 0 can be reset from the external world via the P2 connector, while the remaining TRAM slots can be reset from either the same source as slot 0 or from a sub-system generated by the TRAM in slot 0.

Software

The TMB12 can be programmed with software development packages to run Occam, C, FORTRAN, Pascal and other transputer language compilers as well as Helios, TransIDRIS, Express and other transputer operating systems. It can also be used as the processing hardware for a number of application specific software packages that are available for the transputer.

Ordering Information

PART NUMBER	DESCRIPTION
TMB12	DOUBLE EXTENDED EUROCARD MOTHERBOARD WITH 16 TRAM SLOTS

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Document Reference:TMB12FLY0789

Transtech TTG1

Display Resolutions

The dispaly resolution supported is 512 x 512 8-bit pixels, allowing up to 256 colours from a maximum of 16.7 million (via look up table) on the screen simultaneously. The TTG1 uses the Inmos IMSG178 colour palette device as the colour look up table, having three 6/8 bit DACs (Digital to Analog converters) on chip. To maintain upwards compatibility with the IMSB007 and TSB07, the TTG1 offers software selectable 6/8 bit DAC mode.

In 6-bit mode any 256 from 262144 colours may be displayed. In 8-bit mode, the display allows any 256 from 16.7 million colours.

Separate Red, Green and Blue SMB connectors are available for connection to standard RGB analogue monitors with composite sync on green.

IMSB007 and TSB07 Compatible

The Transtech TTG1 is compatible at software level with the Transtech TSB07 and Inmos IMSB007. A library of relevant routines required for setting up the video timing generator is supplied with the board. These library routines may be used to port existing IMSB007 or TSB07 code to the TTG1.

TRAM Standard

Measuring only 2.10" by 3.66" (5.33mm by 9.30mm) the TTG1 conforms to the published TRAM standard, allowing them to be easily plugged onto a wide range of motherboards for many different host machines. Up to ten TRAMs can be accommodated on a Transtech TMB08 board for IBM PC XT or AT's and compatibles, 4 on the Transtech TMB04 and TMB05, 16 on a TMB12 double extended eurocard and 32 on the MCP1000 Multi Computing Platform for Sun workstations, allowing rapid prototyping of transputer systems. Transtech TRAMs are also compatible with motherboards from other manufacturers. Further details on the TRAM standard and TRAM Module Motherboard Architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

Software

The TTG1 is supported by Occam primitives which generate key graphics functioins callable from the Occam TDS or 3L's scientific languages.

Ordering Information

PART NUMBER	DESCRIPTION
TTG1	TRANSPUTER GRAPHICS TRAM WITH T800-25 AND IMSG178

TRANSTECH DEVICES LIMITED
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Document Reference:TTG1FLY0789

TTG

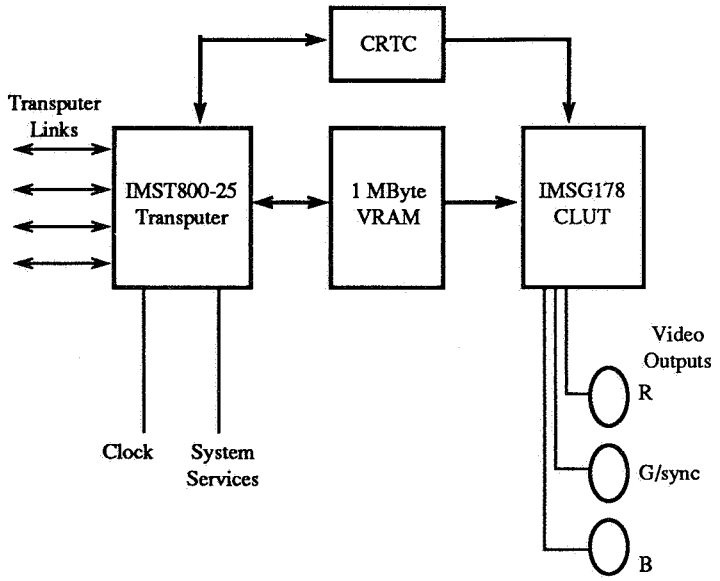
Transtech TRAMs
TTG1

TTG

A TRANSPUTER GRAPHICS MODULE

Features

- **IMST800-25 transputer**
- **1 MByte of video RAM**
- **Supports resolutions upto 512 x 512 8-bit pixels**
- **256 colours from a maximum of 16.7 million**
- **Software selectable 6 or 8-bit DAC mode**
- **Software compatible with the Transtech TSB07 and Inmos IMSB007**
- **Four serial transputer links**
- **Industry standard size 2 TRAM**
- **Compatible with Transtech range of TRAM motherboards**



Introduction

The Transtech TTG1 TRAM (TRAnsputer Module) is a small industry standard daughterboard for the Transtech range of TRAM motherboards. The TTG1 consists of an IMST800-25 floating point transputer with 1 MByte of video memory suitable for user code, data and screen data.

Four Display Windows

The video memory can be treated as up to four independant display windows, each having a resolution of 512 x 512 8-bit pixels. Any one of these windows may be displayed at any time. User code may access any of the windows, including the one currently displayed, the access to the other three windows being invisible to the final display. The choice of display window can be controlled in software. The ability to switch active windows assists animation, where the next frame may be generated whilst the current frame is displayed.

TTG

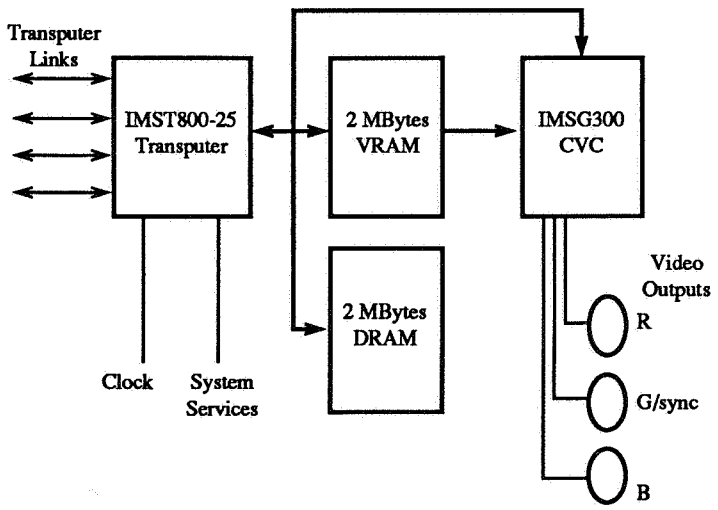
Transtech TRAMs
TTG3

TTG

A HIGH RESOLUTION GRAPHICS MODULE

Features

- **IMST800-25 transputer**
- **IMSG300 CVC (Clour Video Controller)**
- **2 MBytes of video RAM (dual ported)**
- **2 MBytes of dynamic RAM**
- **Supports resolutions upto 1280 x 1024 8-bit pixels**
- **Fast hardware screen clear function**
- **Interleaved memory**
- **Four serial transputer links**
- **Industry standard size 4 TRAM**
- **Compatible with Transtech range of TRAM motherboards**



Introduction

The Transtech TTG3 TRAM (TRAnsputer Module) is a small industry standard daughterboard for the Transtech range of TRAM motherboards. It is the first commercially available product to make use of the new Inmos IMSG300 CVC (colour video controller). The TTG3 consists of an IMST800-25 floating point transputer with 2 MBytes of program memory and 2 MBytes video memory, where the video memory is dual ported and also accessed by the IMSG300 CVC.

IMSG300 Graphics Display

The TTG3 supports resolutions upto 1280 x 1024 8 bit pixels, or two screens of 1024 x 1024 8 bit pixels for double buffered animation applications, displaying 256 colours from a palette of 16.7 million possible colours at a 60 Hz refresh rate. The IMSG300 is a fully programmable display controller consisting of a video timing generator, VRAM interface, on chip colour look up table and three 8 bit DACs (digital to analog converters). The IMSG300 can be programmed by the transputer via memory mapped registers.

Transtech TTG3

Hardware Functions

The TTG3 supports an interleaving mechanism transparent to the user which increases performance when the IMST800 is accessing contiguous blocks of memory. The IMST800 has full read and write control over the video memory. A fast screen clear function in hardware enables the entire video memory to be cleared in less than 0.5 ms, or for a band on the screen to be cleared to any colour at less than 1 us per pixel. Separate Red, Green and Blue SMB connectors are available for connection to standard RGB analogue monitors with composite sync on green, as well as separate sync available on headers.

TRAM Standard

Measuring only 4.20" by 3.66" (10.66mm by 9.30mm) the TTG3 conforms to the published TRAM standard, allowing them to be easily plugged onto a wide range of motherboards for many different host machines. Up to 10 TRAMs can be accommodated on a Transtech TMB08 board for IBM PC XT or AT's and compatibles, 4 on the Transtech TMB04 and TMB05, 16 on a TMB12 double extended eurocard and 32 on the MCP1000 Multi Computing Platform for Sun workstations, allowing rapid prototyping of transputer systems. Transtech TRAMs are also compatible with motherboards from other manufacturers. Further details on the TRAM standard and TRAM Module Motherboard Architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

Software

The TTG3 is supported by Occam primitives which generate key graphics functioins callable from the Occam TDS or 3L's scientific languages. The board will also support the X windows environment. This allows the TTG3 to implement graphics primitves directly or to act as an intelligent channel receiving data via the transputer serial links.

Ordering Information

PART NUMBER	DESCRIPTION
TTG3	HIGH RESOLUTION GRAPHICS TRAM WITH T800-25 AND G300

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Document Reference:TTG3FLY0789

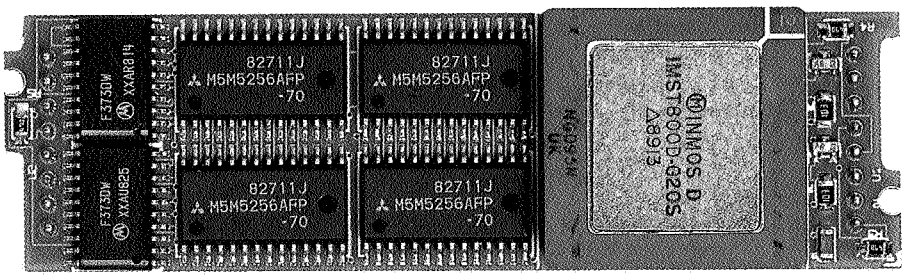
TTM

Transtech TRAMs TTM1 and TTM2

TTM

Features

- **IMST800, IMST425 or IMST414 transputer options**
- **32 or 128 KBytes of static RAM**
- **Zero wait state memory**
- **Four serial transputer links**
- **Only 16 active pins**
- **Industry standard size 1 TRAM**
- **Compatible with Transtech range of TRAM motherboards**
- **Full Sub-system control**



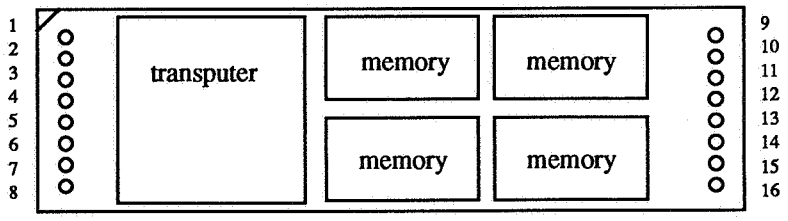
Introduction The Transtech TTM1 and TTM2 TRAMs (TRAnsputer Modules) are small industry standard daughterboards for the Transtech range of TRAM motherboards. They have 32 or 128 KBytes of static RAM respectively and are capable of supporting the IMST800, IMST425 and IMST414 transputers.

TRAM Standard Measuring only 1.05" by 3.66" (2.67mm by 9.30mm) the TTM1 and TTM2 conform to the published TRAM standard, allowing them to be plugged easily onto a wide range of motherboards for many different host machines. Up to 10 TRAMs can be accommodated on a Transtech TMB08 board for IBM PC XT or AT's and compatibles, 4 on the Transtech TMB04 and TMB05, 16 on a TMB12 double extended eurocard and 32 on the MCP1000 Multi Computing Platform for Sun workstations, allowing rapid prototyping of transputer systems. Transtech TRAMs are also compatible with motherboards from other manufacturers. Further details on the TRAM standard and TRAM Module Motherboard Architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

Transtech TTM1 and TTM2

Functional Description

TRAMs use 16 pins for communication with the motherboard and for obtaining power. However, TRAMs that are larger than size 1 have more than 16 pins, with the extra pins providing more power and ground connections. The extra pins also propagate the signals from the motherboard below to allow stacking of modules. The link speed of the TRAMs is selected by two pins. When both are held low the links operate at 10 Mbits/sec and when high at 20 Mbits/sec. This is implemented by jumpers or switches on the motherboards. The allocation of the pins are shown in the following diagram.



1 Link2Out	9 Link3In
2 Link2In	10 Link3Out
3 VCC	11 GND
4 Link1Out	12 Link0In
5 Link1In	13 Link0Out
6 LinkSpeedA	14 notError
7 LinkSpeedB	15 Reset
8 ClockIn(5MHz)	16 Analyse

Ordering Information

Part Number	Processor Type	Processor Cycle Time (ns)	Memory (KBytes)	Memory CycleTime (ns)
TTM1-4	IMST414-20	50	32	150
TTM1-42	IMST425-20	50	32	150
TTM1-8	IMST800-20	50	32	150
TTM2-4	IMST414-20	50	128	150
TTM2-42	IMST425-20	50	128	150
TTM2-8	IMST800-20	50	128	150

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Document Reference:TTM1&2FLY0789

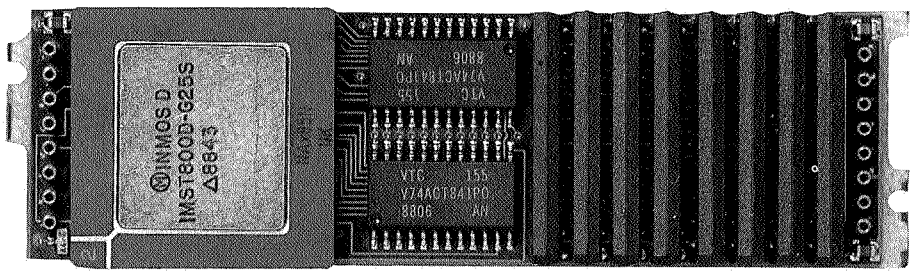
TTM

Transtech TRAMs
TTM3

TTM

Features

- **IMST800, IMST425 or IMST414 transputer options**
- **1 MByte of dynamic RAM**
- **Zero wait state memory option**
- **20, 25 or 30 MHz transputer speed option**
- **Four serial transputer links**
- **Only 16 active pins**
- **Industry standard size 1 TRAM**
- **Compatible with Transtech range of TRAM motherboards**



Introduction The Transtech TTM3 TRAM (TRAnsputer Module) is a small industry standard daughterboard for the Transtech range of TRAM motherboards. It has 1 MByte of dynamic RAM and is capable of supporting the IMST800, IMST425 and IMST414 transputers.

TRAM Standard Measuring only 1.05" by 3.66" (2.67mm by 9.30mm) the TTM3 conforms to the published TRAM standard, allowing them to be plugged easily onto a wide range of motherboards for many different host machines. Up to 10 TRAMs can be accommodated on a Transtech TMB08 board for IBM PC XT or AT's and compatibles, 4 on the Transtech TMB04 and TMB05, 16 on a TMB12 double extended eurocard and 32 on the MCP1000 Multi Computing Platform for Sun workstations, allowing rapid prototyping of transputer systems. Transtech TRAMs are also compatible with motherboards from other manufacturers. Further details on the TRAM standard and TRAM Module Motherboard Architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

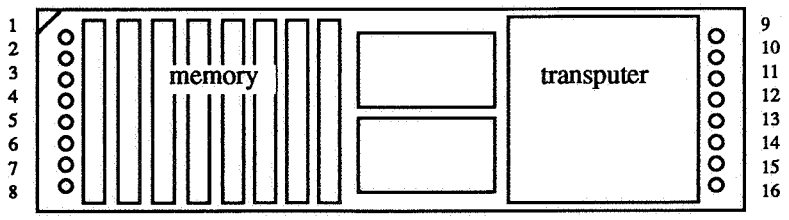
TTM

Transtech TTM3

TTM

Functional Description

TRAMs use 16 pins for communication with the motherboard and for obtaining power. However, TRAMs that are larger than size 1 have more than 16 pins, with the extra pins providing more power and ground connections. The extra pins also propagate the signals from the motherboard below to allow stacking of modules. The link speed of the TRAMs is selected by two pins. When both are held low the links operate at 10 Mbits/sec and when high at 20 Mbits/sec. This is implemented by jumpers or switches on the motherboards. The allocation of the pins are shown in the following diagram.



1 Link2Out	9 Link3In
2 Link2In	10 Link3Out
3 VCC	11 GND
4 Link1Out	12 Link0In
5 Link1In	13 Link0Out
6 LinkSpeedA	14 notError
7 LinkSpeedB	15 Reset
8 ClockIn(5MHz)	16 Analyse

Ordering Information

Part Number	Processor Type	Processor Cycle Time (ns)	Memory (MBytes)	Memory CycleTime (ns)
TTM3-4	IMST414-20	50	1	200
TTM3-42	IMST425-20	50	1	200
TTM3-8	IMST800-20	50	1	200
TTM3-8-F	IMST800-20	50	1	150
TTM3-85	IMST800-25	40	1	160
TTM3-85-F	IMST800-25	40	1	120
TTM3-830	IMST800-30	33	1	132

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Document Reference:TTM3FLY0789

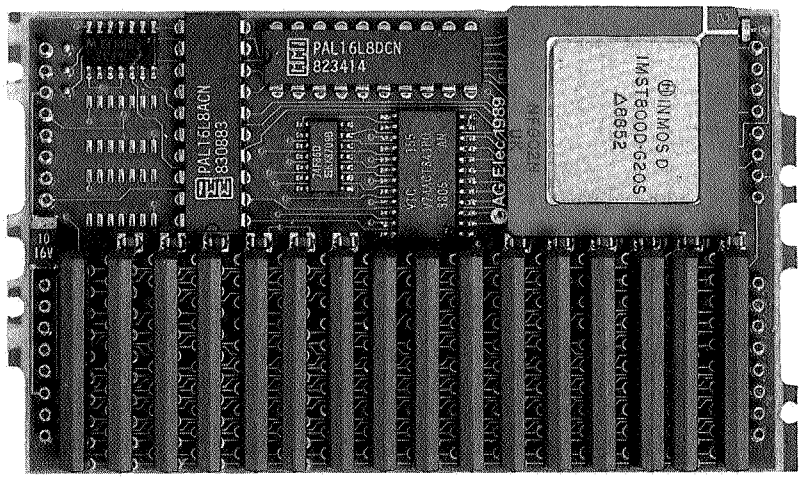
TTM

Transtech TRAMs
TTM6

TTM

Features

- **IMST800, IMST425 or IMST414 transputer options**
- **2 MBytes of dynamic RAM**
- **Zero wait state memory option**
- **20, 25 or 30 MHz transputer speed option**
- **Four serial transputer links**
- **Only 16 active pins**
- **Industry standard size 2 TRAM**
- **Compatible with Transtech range of TRAM motherboards**
- **Full Sub-system control**



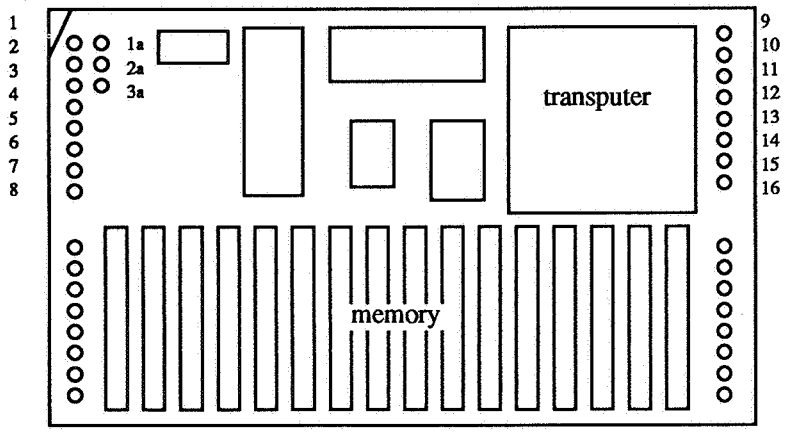
Introduction The Transtech TTM6 TRAM (TRAnsputer Module) is a small industry standard daughterboard for the Transtech range of TRAM motherboards. It has 2 MBytes of dynamic RAM and is capable of supporting the IMST800, IMST425 and IMST414 transputers. It also has the ability to control a sub-system of transputers.

TRAM Standard Measuring only 2.10" by 3.66" (5.33mm by 9.30mm) the TTM6 conforms to the published TRAM standard, allowing them to be plugged easily onto a wide range of motherboards for many different host machines. Up to 10 TRAMs can be accommodated on a Transtech TMB08 board for IBM PC XT or AT's and compatibles, 4 on the Transtech TMB04 and TMB05, 16 on a TMB12 double extended eurocard and 32 on the MCP1000 Multi Computing Platform, allowing rapid prototyping of transputer systems. Transtech TRAMs are also compatible with motherboards from other manufacturers. Further details on the TRAM standard and TRAM Module Motherboard Architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

Transtech TTM6

Functional Description

TRAMs use 16 pins for communication with the motherboard and for obtaining power. However, TRAMs that are larger than size 1 have more than 16 pins, with the extra pins providing more power and ground connections. The extra pins also propagate the signals from the motherboard below to allow stacking of modules. The link speed of the TRAMs is selected by two pins. When both are held low the links operate at 10 Mbits/sec and when high at 20 Mbits/sec. This is implemented by jumpers or switches on the motherboards. The allocation of the pins are shown in the following diagram.



1 Link2Out	9 Link3In
2 Link2In	10 Link3Out
3 VCC	11 GND
4 Link1Out	12 Link0In
5 Link1In	13 Link0Out
6 LinkSpeedA	14 notError
7 LinkSpeedB	15 Reset
8 ClockIn(5MHz)	16 Analyse

Ordering Information

Part Number	Processor Type	Processor Cycle Time (ns)	Memory (MBytes)	Memory CycleTime (ns)
TTM6-4	IMST414-20	50	2	200
TTM6-42	IMST425-20	50	2	200
TTM6-8	IMST800-20	50	2	200
TTM6-8-F	IMST800-20	50	2	150
TTM6-85	IMST800-25	40	2	160
TTM6-85-F	IMST800-25	40	2	120
TTM6-830	IMST800-30	33	2	132

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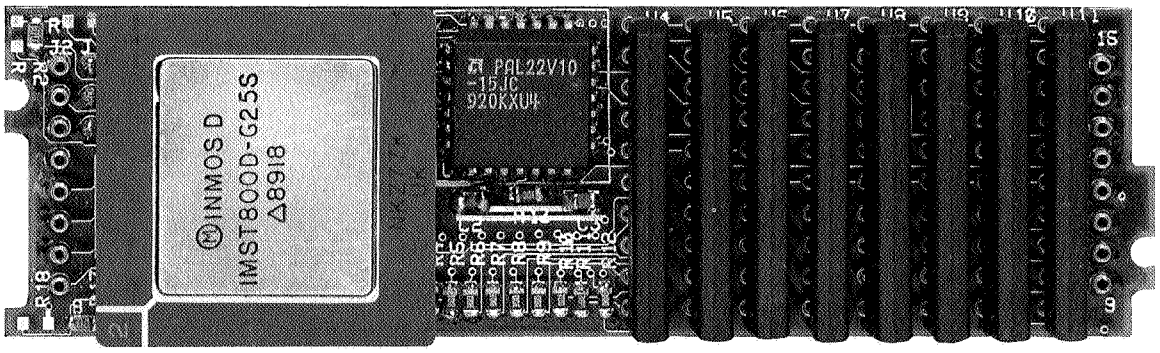
TTM

Transtech TRAMs
TTM7

TTM

Features

- **IMST800, IMST425 or IMST414 transputer options**
- **1 MByte of dynamic RAM**
- **Zero wait state memory option**
- **20, 25 or 30 MHz transputer speed option**
- **Four serial transputer links**
- **Only 16 active pins**
- **Industry standard size 1 TRAM**
- **Compatible with Transtech range of TRAM motherboards**
- **Full sub-system control**



Introduction

The Transtech TTM7 TRAM (TRAnsputer Module) is a small industry standard daughterboard for the Transtech range of TRAM motherboards. It has 1 MByte of dynamic RAM and is capable of supporting the IMST800, IMST425 and IMST414 transputers. It is also capable of controlling a sub-system of transputers.

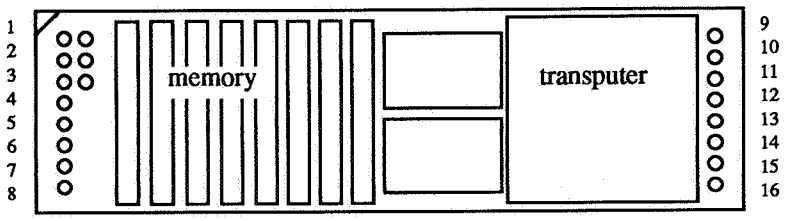
TRAM Standard

Measuring only 1.05" by 3.66" (2.67mm by 9.30mm) the TTM7 conforms to the published TRAM standard, allowing them to be plugged easily onto a wide range of motherboards for many different host machines. Up to 10 TRAMs can be accommodated on a Transtech TMB08 board for IBM PC XT or AT's and compatibles, 4 on the Transtech TMB04 and TMB05, 16 on a TMB12 double extended eurocard and 32 on the MCP1000 Multi Computing Platform for Sun workstations, allowing rapid prototyping of transputer systems. Transtech TRAMs are also compatible with motherboards from other manufacturers. Further details on the TRAM standard and TRAM Module Motherboard Architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

Transtech TTM7

Functional Description

TRAMs use 16 pins for communication with the motherboard and for obtaining power. However, TRAMs that are larger than size 1 have more than 16 pins, with the extra pins providing more power and ground connections. The extra pins also propagate the signals from the motherboard below to allow stacking of modules. The link speed of the TRAMs is selected by two pins. When both are held low the links operate at 10 Mbits/sec and when high at 20 Mbits/sec. This is implemented by jumpers or switches on the motherboards. The allocation of the pins are shown in the following diagram.



1 Link2Out	9 Link3In
2 Link2In	10 Link3Out
3 VCC	11 GND
4 Link1Out	12 Link0In
5 Link1In	13 Link0Out
6 LinkSpeedA	14 notError
7 LinkSpeedB	15 Reset
8 ClockIn(5MHz)	16 Analyse

Ordering Information

Part Number	Processor Type	Processor Cycle Time (ns)	Memory (MBytes)	Memory CycleTime (ns)
TTM7-4	IMST414-20	50	1	200
TTM7-42	IMST425-20	50	1	200
TTM7-8	IMST800-20	50	1	200
TTM7-8-F	IMST800-20	50	1	150
TTM7-85	IMST800-25	40	1	160
TTM7-85-F	IMST800-25	40	1	120
TTM7-830	IMST800-30	33	1	132

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TTM

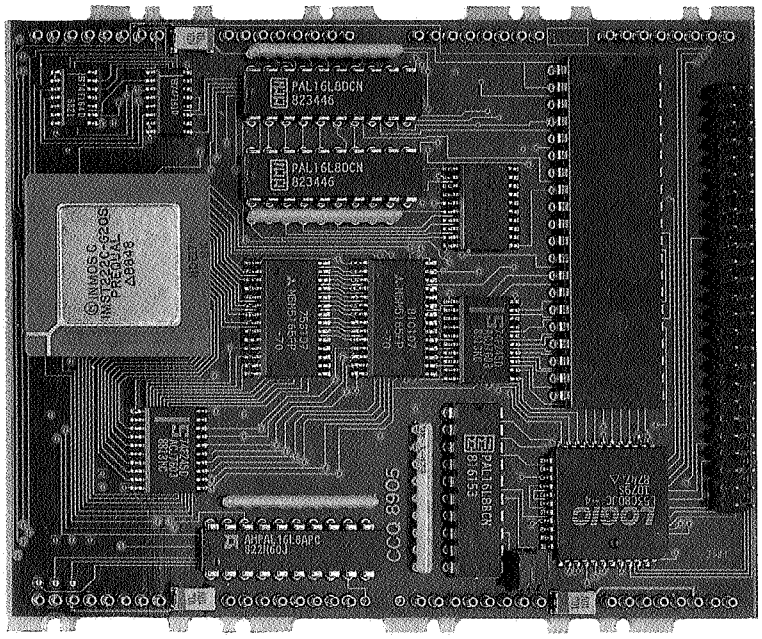
Transtech TRAMs
TTM11

TTM

A SCSI INTERFACE TRANSPUTER MODULE

Features

- **IMST222 16-bit transputer**
- **1.8 MBytes/sec data rate over SCSI bus**
- **Extendable to multi master, multi slave system**
- **Software support with TBIOS disk filing system**
- **Industry standard size 4 TRAM**
- **Compatible with Transtech range of TRAM motherboards**



Introduction The Transtech TTM11 is a small daughterboard for the Transtech range of TRAM (TRAnsputer Module) motherboards. It comprises an IMST222 16-bit transputer with 64K of fast static RAM interfaced to a Logic Devices SCSI controller. Data throughput is determined by a single Inmos link bandwidth, typically of the order of 1.2 MBytes/sec, although the SCSI bus side of the module will transfer at data rates of upto 1.8 MBytes/sec.

TRAM Standard Measuring only 4.20" by 3.66" (10.67mm x 9.30mm) the TTM11 conforms to the published TRAM standard, allowing it to be plugged easliy onto a wide range of motherboards for many different host machines. Up to 10 TRAMs can be accommodated on a Transtech TMB08 board for IBM PC XT or AT's and compatibles, 4 on the Transtech TMB04 and TMB05, 16 on a TMB12 double extended eurocard and 32 on the MCP1000 Multi Computing Platform for Sun workstations, allowing rapid prototyping of transputer systems. The TTM11 is compatible with TRAM motherboards from Transtech and also those from other manufacturers. Further details on the TRAM standard and TRAM motherboard architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

Transtech TTM11

Software

TBIOS (Transputer BIOS) is a library of Occam routines provided to access the SCSI bus from an application program running on a network of transputers.

Software developers using Occam, can include the TBIOS as a library function to provide fast and efficient access to mass storage on the SCSI bus. Alternatively the use of TDOS which comprises the TBIOS routines provides a shell from which to run applications such as the TDS (Transputer Development System). Full listings of Occam examples to interface to the TBIOS are provided.

Users of the 3L scientific languages can run TBIOS as a separate task, and use channel communication from their application to access the mass store directly, without going through layers of unwieldly protocols. Examples are provided in each language to emulate the required primitives open, read, write and close file structured I/O. These primitives are implemented in as near a 'look alike' form as the inherent language primitives to allow simple mass editing of existing code to run under this system.

A RAMDISK utility provided with the TBIOS allows the user to create automatic caching of files to memory without major program changes.

EPROM Bootable

The TTM11 can be used to boot a network of transputers from the SCSI port when used in conjunction with the TTM12 EPROM loader TRAM which boots the T222 transputer. For more details see information on the Transtech TTM12 TRAM.

PART NUMBER	DESCRIPTION
TTM11	TRANSPUTER SCSI INTERFACE MODULE

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Document Reference:TTM11FLY0789

TTM

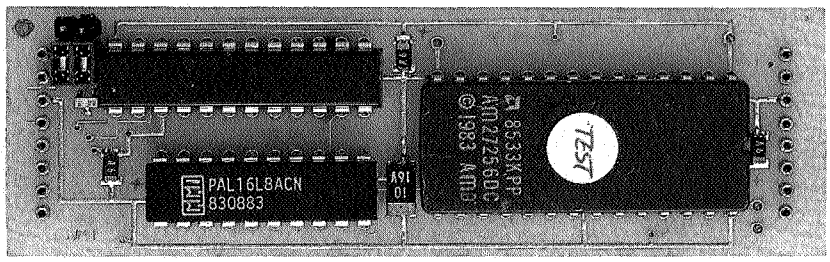
Transtech TRAMs
TTM12

TTM

EPROM LOADER/BOOTSTRAP TRAM

Features

- **Up to 27512 EPROM (64 KBytes)**
- **Plugs directly onto other TRAMs**
- **IMSC012 link adaptor**
- **Allows standalone systems to be rapidly built**
- **Size 1 TRAM**
- **Compatible with Transtech TTM11 SCSI TRAM**
- **Compatible with Transtech range of TRAM motherboards**



Introduction The Transtech TTM12 is a small daughterboard for the Transtech range of TRAM (TRAnsputer Module) motherboards, that allows a transputer system to be made standalone from a development system. The TTM12 has a 27512 EPROM which can be programmed to hold transputer boot code to be downloaded through a link on reset. The EPROM can be loaded with code developed by any transputer development system, using a suitable PROM programming system.

TRAM Standard Measuring only 1.05" by 3.66" (2.67mm x 9.30mm) the TTM12 conforms to the published TRAM standard allowing it to be plugged easily onto a wide range of motherboards (or TRAMs) from Transtech and other manufacturers. Up to 10 TRAMs can be accommodated on a Transtech TMB08 board for IBM PC XT or AT's and compatibles, 4 on the Transtech TMB04 and TMB05, 16 on a TMB12 double extended eurocard and 32 on the MCP1000 Multi Computing Platform for Sun workstations, allowing rapid prototyping of transputer systems. Transtech TRAMs are also compatible with motherboards from other manufacturers. Further details on the TRAM standard and TRAM Module Motherboard Architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

Transtech TTM12

Functional Description

The TTM12 can output code on either link 1 or link 2 (selectable by jumper), allowing the transputer to which it is attached to be booted from ROM while it is set to boot from link. This has the advantage that TRAMs (that are normally fixed to boot from link) can be booted in a standalone system without the need to build any special hardware. The TTM12 outputs code immediately after the end of a reset and should be at the same level in the system services hierarchy as the processor which it is intended to boot. The links on the TTM12 can be set to run at 10 or 20 Mbits/sec to enable it to support systems using either link speed. The capability of selecting either link 1 or link 2 enables the TTM12 to be connected to either 'pipehead' or 'pipetail' in TRAM systems.

Booting systems via a SCSI interface

When the TTM12 is used in conjunction with the Transtech TTM11 SCSI interface TRAM it enables an entire system to be booted. The TTM12 can boot the IMST222 16-bit transputer on the TTM11 with a program that causes the TTM11 to load code stored on a SCSI disk to the rest of the transputer network. In this case the TTM12 is stacked on top of the TTM11 so that it is directly connected to it without having to use connections on the motherboard. It must be remembered not to connect another TRAM to the link being used to boot the TTM11. For more details see information on the Transtech TTM11 SCSI interface TRAM.

Ordering Information

PART NUMBER	DESCRIPTION
TTM12	EPROM LOADER/BOOTSTRAP TRAM

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Document Reference:TTM12FLY0789

TTM

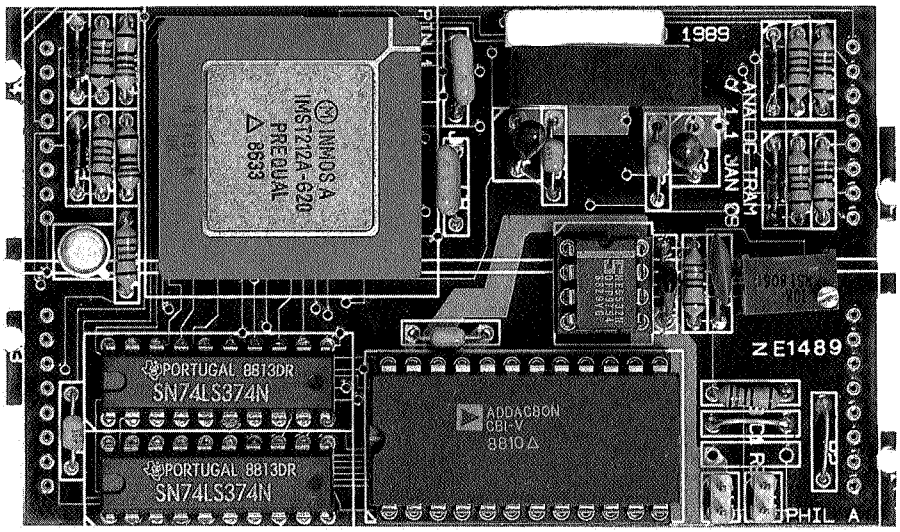
Transtech TRAMs
TTM14

TTM

A DIGITAL TO ANALOG CONVERTER TRAM

Features

- **IMST212 16-bit transputer**
- **12-bit D to A converter**
- **Analog output channel**
- **Standard size 2 TRAM**



Introduction

The TTM14 is a small daughterboard for the Transtech range of TRAM (TRAnsputer Module) motherboards. It has an IMST212 16-bit transputer interfaced to a 12-bit digital to analog converter. The TTM14's single analog output channel enables transputer systems to generate a high quality analog signal for use in robotics, process control, waveform generation, digital audio,speech synthesis and similar applications.

TRAM Standard

Measuring only 2.10" by 3.66" (5.33mm by 9.30mm) the TTM14 conforms to the published TRAM standard, allowing them to be plugged easily onto a wide range of motherboards for many different host machines. Up to 10 TRAMs can be accommodated on a Transtech TMB08 board for IBM PC XT or AT's and compatibles, 4 on the Transtech TMB04 and TMB05, 16 on a TMB12 double extended eurocard and 32 on the MCP1000 Multi Computing Platform for Sun workstations, allowing rapid prototyping of transputer systems. Transtech TRAMs are also compatible with motherboards from other manufacturers. Further details on the TRAM standard and TRAM Module Motherboard Architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

Transtech TTM14

Functional Description

Several TTM14's may be used in a TRAM based system to perform multi-channel control. The IMST212 transputer has enough memory and processing power to perform sophisticated digital signal processing on digital output data. The software provided with the TTM14 demonstrates how the T212 can be used to directly output data it has received on its links, or run a more complicated program controlled by an IMST800, IMST425 or IMST414 transputer. The IMST212 may be replaced by an IMST222 if more memory is required.

From an analog point of view the board is extremely flexible. The analog output frequency response is controlled by resistors and capacitors, and is presented in both unbuffered and low pass filtered form. The analog buffer is socketed and has a standard pin out, to enable it to be replaced by a device with other qualities such as lower offset voltage or lower output impedance. When shipped the TTM14 has a filter cut off frequency of 15 KHz and a 10us maximum slew rate.

Ordering Information

PART NUMBER	DESCRIPTION
TTM14	DIGITAL TO ANALOG CONVERTER TRAM

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Document Reference:TTM14FLY0789

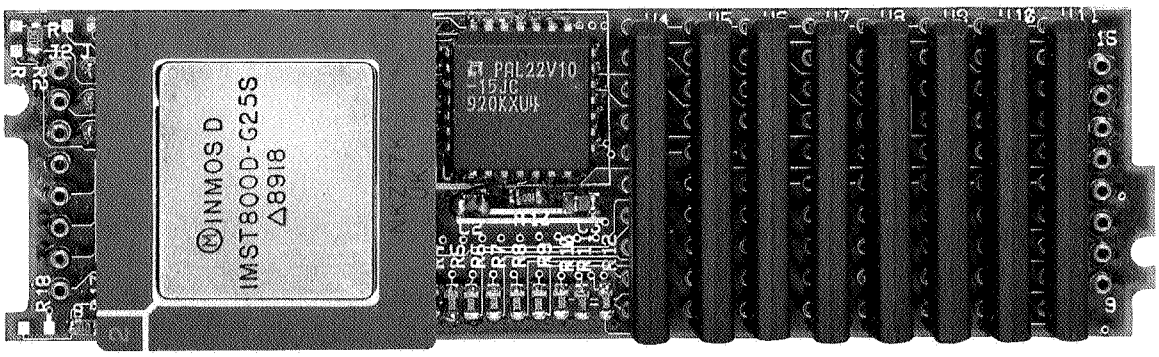
TTM

Transtech TRAMs
TTM15

TTM

Features

- **IMST800, IMST425 or IMST414 transputer options**
- **4 MBytes of dynamic RAM**
- **Zero wait state memory option**
- **20, 25 or 30 MHz transputer speed option**
- **Four serial transputer links**
- **Only 16 active pins**
- **Industry standard size 1 TRAM**
- **Compatible with Transtech range of TRAM motherboards**
- **Full sub-system control, allows operation as a Master**



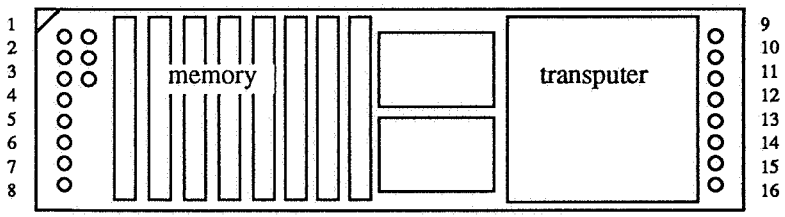
Introduction The Transtech TTM15 TRAM (TRAnsputer Module) is a small industry standard daughterboard for the Transtech range of TRAM motherboards. It has 4 MBytes of dynamic RAM and is capable of supporting the IMST800, IMST425 and IMST414 transputers. It also has the ability to control a sub-system of transputers.

TRAM Standard Measuring only 1.05" by 3.66" (2.67mm by 9.30mm) the TTM15 conforms to the published TRAM standard, allowing them to be plugged easily onto a wide range of motherboards for many different host machines. Up to 10 TRAMs can be accommodated on a Transtech TMB08 board for IBM PC XT or AT's and compatibles, 4 on the Transtech TMB04 and TMB05, 16 on a TMB12 double extended eurocard and 32 on the MCP1000 Multi Computing Platform for Sun workstations, allowing rapid prototyping of transputer systems. Transtech TRAMs are also compatible with motherboards from other manufacturers. Further details on the TRAM standard and TRAM Module Motherboard Architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

Transtech TTM15

Functional Description

TRAMs use 16 pins for communication with the motherboard and for obtaining power. However, TRAMs that are larger than size 1 have more than 16 pins, with the extra pins providing more power and ground connections. The extra pins also propagate the signals from the motherboard below to allow stacking of modules. The link speed of the TRAMs is selected by two pins. When both are held low the links operate at 10 Mbits/sec and when high at 20 Mbits/sec. This is implemented by jumpers or switches on the motherboards. The allocation of the pins are shown in the following diagram.



1 Link2Out	9 Link3In
2 Link2In	10 Link3Out
3 VCC	11 GND
4 Link1Out	12 Link0In
5 Link1In	13 Link0Out
6 LinkSpeedA	14 notError
7 LinkSpeedB	15 Reset
8 ClockIn(5MHz)	16 Analyse

Ordering Information

Part Number	Processor Type	Processor Cycle Time (ns)	Memory (MBytes)	Memory CycleTime (ns)
TTM15-4-F	IMST414-20	50	4	150
TTM15-42-F	IMST425-20	50	4	150
TTM15-8-F	IMST800-20	50	4	150
TTM15-85	IMST800-25	40	4	160
TTM15-85-F	IMST800-25	40	4	120
TTM15-830	IMST800-30	33	4	132

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Document Reference:TTM15FLY0889

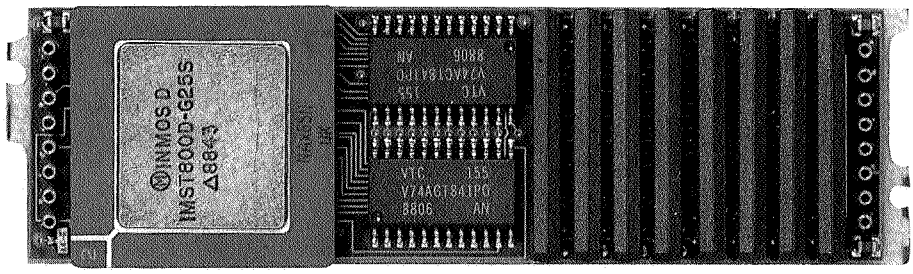
TTM

Transtech TRAMs
TTM16

TTM

Features

- **IMST800, IMST425 or IMST414 transputer options**
- **4 MBytes of dynamic RAM**
- **Zero wait state memory option**
- **20, 25 or 30 MHz transputer speed option**
- **Four serial transputer links**
- **Only 16 active pins**
- **Industry standard size 1 TRAM**
- **Compatible with Transtech range of TRAM motherboards**



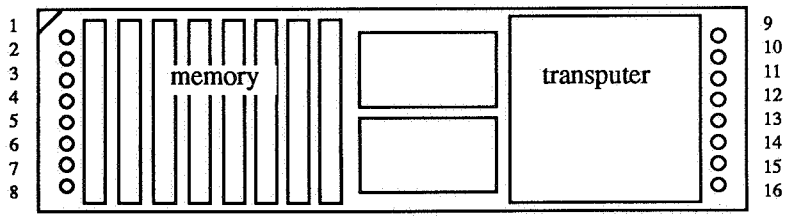
Introduction The Transtech TTM16 TRAM (TRAnsputer Module) is a small industry standard daughterboard for the Transtech range of TRAM motherboards. It has 4 MBytes of dynamic RAM and is capable of supporting the IMST800, IMST425 and IMST414 transputers.

TRAM Standard Measuring only 1.05" by 3.66" (2.67mm by 9.30mm) the TTM16 conforms to the published TRAM standard, allowing them to be plugged easily onto a wide range of motherboards for many different host machines. Up to 10 TRAMs can be accommodated on a Transtech TMB08 board for IBM PC XT or AT's and compatibles, 4 on the Transtech TMB04 and TMB05, 16 on a TMB12 double extended eurocard and 32 on the MCP1000 Multi Computing Platform for Sun workstations, allowing rapid prototyping of transputer systems. Transtech TRAMs are also compatible with motherboards from other manufacturers. Further details on the TRAM standard and TRAM Module Motherboard Architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

Transtech TTM16

Functional Description

TRAMs use 16 pins for communication with the motherboard and for obtaining power. However, TRAMs that are larger than size 1 have more than 16 pins, with the extra pins providing more power and ground connections. The extra pins also propagate the signals from the motherboard below to allow stacking of modules. The link speed of the TRAMs is selected by two pins. When both are held low the links operate at 10 Mbits/sec and when high at 20 Mbits/sec. This is implemented by jumpers or switches on the motherboards. The allocation of the pins are shown in the following diagram.



1 Link2Out	9 Link3In
2 Link2In	10 Link3Out
3 VCC	11 GND
4 Link1Out	12 Link0In
5 Link1In	13 Link0Out
6 LinkSpeedA	14 notError
7 LinkSpeedB	15 Reset
8 ClockIn(5MHz)	16 Analyse

Ordering Information

Part Number	Processor Type	Processor Cycle Time (ns)	Memory (MBytes)	Memory CycleTime (ns)
TTM16-4-F	IMST414-20	50	4	150
TTM16-42-F	IMST425-20	50	4	150
TTM16-8-F	IMST800-20	50	4	150
TTM16-85	IMST800-25	40	4	160
TTM16-85-F	IMST800-25	40	4	120
TTM16-830	IMST800-30	33	4	132

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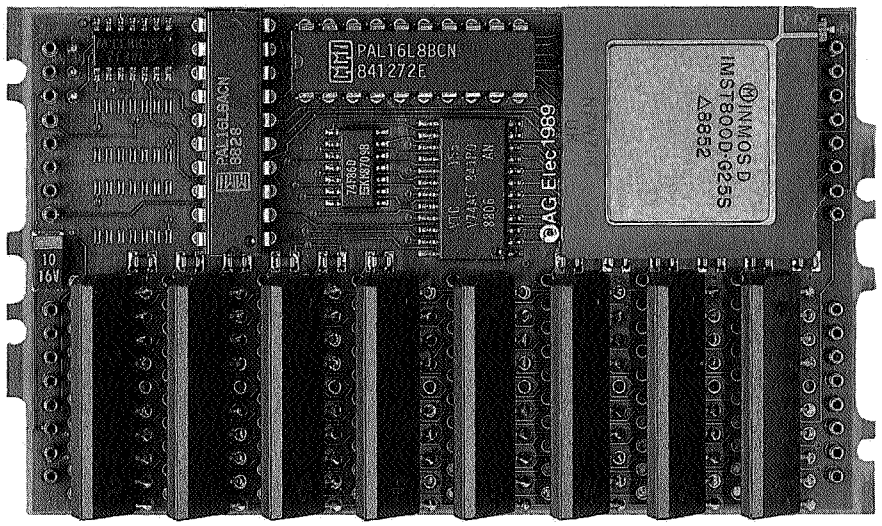
TTM

Transtech TRAMs
TTM17

TTM

Features

- **IMST800, IMST425 or IMST414 transputer options**
- **4 MBytes of dynamic RAM**
- **Zero wait state memory option**
- **20, 25 or 30 MHz transputer speed option**
- **Four serial transputer links**
- **Only 16 active pins**
- **Industry standard size 2 TRAM**
- **Compatible with Transtech range of TRAM motherboards**
- **Full Sub-system control**



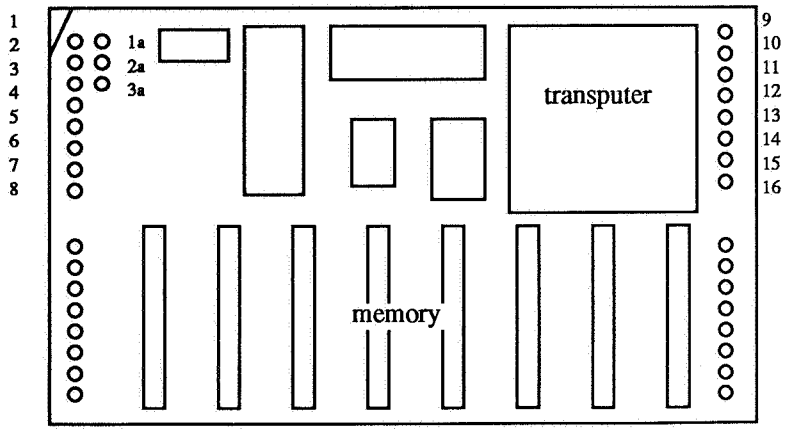
Introduction The Transtech TTM17 TRAM (TRAnsputer Module) is a small industry standard daughterboard for the Transtech range of TRAM motherboards. It has 4 MBytes of dynamic RAM and is capable of supporting the IMST800, IMST425 and IMST414 transputers. It also has the ability to control a sub-system of transputers. The TTM17 is upgradable to 8 MBytes of dynamic RAM by adding extra 4 Mbit ZIP RAM chips.

TRAM Standard Measuring only 2.10" by 3.66" (5.33mm by 9.30mm) the TTM17 conforms to the published TRAM standard, allowing them to be plugged easily onto a wide range of motherboards for many different host machines. Up to 10 TRAMs can be accommodated on a Transtech TMB08 board for IBM PC XT or AT's and compatibles, 4 on the Transtech TMB04 and TMB05, 16 on a TMB12 double extended eurocard and 32 on the MCP1000 Multi Computing Platform, allowing rapid prototyping of transputer systems. Transtech TRAMs are also compatible with motherboards from other manufacturers. Further details on the TRAM standard and TRAM Module Motherboard Architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

Transtech TTM17

Functional Description

TRAMs use 16 pins for communication with the motherboard and for obtaining power. However, TRAMs that are larger than size 1 have more than 16 pins, with the extra pins providing more power and ground connections. The extra pins also propagate the signals from the motherboard below to allow stacking of modules. The link speed of the TRAMs is selected by two pins. When both are held low the links operate at 10 Mbits/sec and when high at 20 Mbits/sec. This is implemented by jumpers or switches on the motherboards. The allocation of the pins are shown in the following diagram.



1 Link2Out	9 Link3In
2 Link2In	10 Link3Out
3 VCC	11 GND
4 Link1Out	12 Link0In
5 Link1In	13 Link0Out
6 LinkSpeedA	14 notError
7 LinkSpeedB	15 Reset
8 ClockIn(5MHz)	16 Analyse

Ordering Information

Part Number	Processor Type	Processor Cycle Time (ns)	Memory (MBytes)	Memory CycleTime (ns)
TTM17-4-F	IMST414-20	50	4	150
TTM17-42-F	IMST425-20	50	4	150
TTM17-8-F	IMST800-20	50	4	150
TTM17-85	IMST800-25	40	4	160
TTM17-85-F	IMST800-25	40	4	120
TTM17-830	IMST800-30	33	4	132

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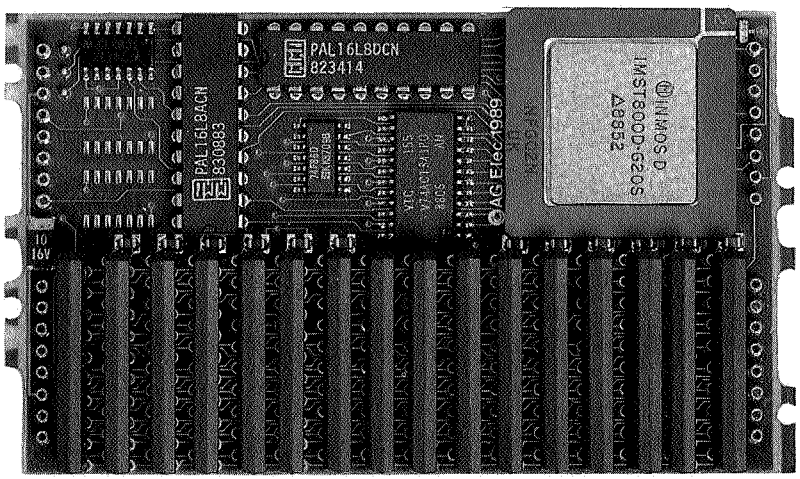
TTM

Transtech TRAMs
TTM18

TTM

Features

- **IMST800, IMST425 or IMST414 transputer options**
- **8 MBytes of dynamic RAM**
- **Zero wait state memory option**
- **20, 25 or 30 MHz transputer speed option**
- **Four serial transputer links**
- **Only 16 active pins**
- **Industry standard size 2 TRAM**
- **Compatible with Transtech range of TRAM motherboards**
- **Full Sub-system control**



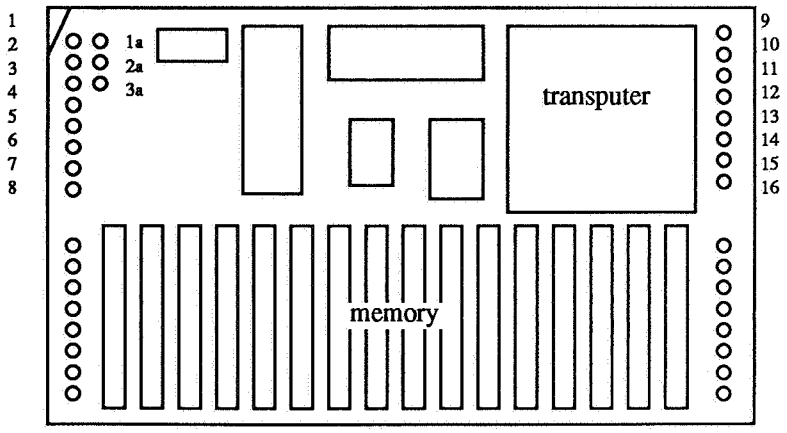
Introduction The Transtech TTM18 TRAM (TRAnsputer Module) is a small industry standard daughterboard for the Transtech range of TRAM motherboards. It has 8 MBytes of dynamic RAM and is capable of supporting the IMST800, IMST425 and IMST414 transputers. It also has the ability to control a sub-system of transputers.

TRAM Standard Measuring only 2.10" by 3.66" (5.33mm by 9.30mm) the TTM18 conforms to the published TRAM standard, allowing them to be plugged easily onto a wide range of motherboards for many different host machines. Up to 10 TRAMs can be accommodated on a Transtech TMB08 board for IBM PC XT or AT's and compatibles, 4 on the Transtech TMB04 and TMB05, 16 on a TMB12 double extended eurocard and 32 on the MCP1000 Multi Computing Platform, allowing rapid prototyping of transputer systems. Transtech TRAMs are also compatible with motherboards from other manufacturers. Further details on the TRAM standard and TRAM Module Motherboard Architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

Transtech TTM18

Functional Description

TRAMs use 16 pins for communication with the motherboard and for obtaining power. However, TRAMs that are larger than size 1 have more than 16 pins, with the extra pins providing more power and ground connections. The extra pins also propagate the signals from the motherboard below to allow stacking of modules. The link speed of the TRAMs is selected by two pins. When both are held low the links operate at 10 Mbits/sec and when high at 20 Mbits/sec. This is implemented by jumpers or switches on the motherboards. The allocation of the pins are shown in the following diagram.



1 Link2Out	9 Link3In
2 Link2In	10 Link3Out
3 VCC	11 GND
4 Link1Out	12 Link0In
5 Link1In	13 Link0Out
6 LinkSpeedA	14 notError
7 LinkSpeedB	15 Reset
8 ClockIn(5MHz)	16 Analyse

Ordering Information

Part Number	Processor Type	Processor Cycle Time (ns)	Memory (MBytes)	Memory CycleTime (ns)
TTM18-4-F	IMST414-20	50	8	150
TTM18-42-F	IMST425-20	50	8	150
TTM18-8-F	IMST800-20	50	8	150
TTM18-85	IMST800-25	40	8	160
TTM18-85-F	IMST800-25	40	8	120
TTM18-830	IMST800-30	33	8	132

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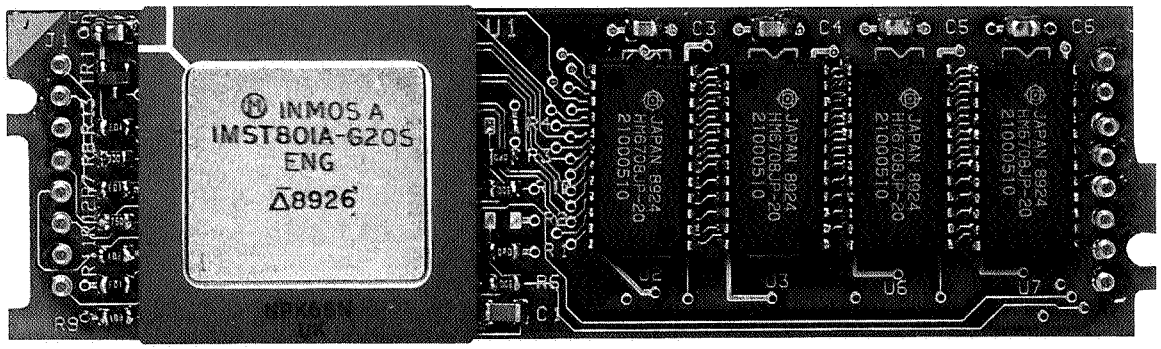
High Performance T801 TRAM Transtech TTM30

Features

- **IMST801 running at 20, 25 or 30 MHz**
- **256 KBytes fast static RAM**
- **Non multiplexed external memory interface**
- **2 processor cycle external memory access (minimum 67 ns)**
- **Four serial transputer links**
- **Only 16 active pins**
- **Industry standard size 1 TRAM**
- **Compatible with Transtech range of TRAM motherboards**



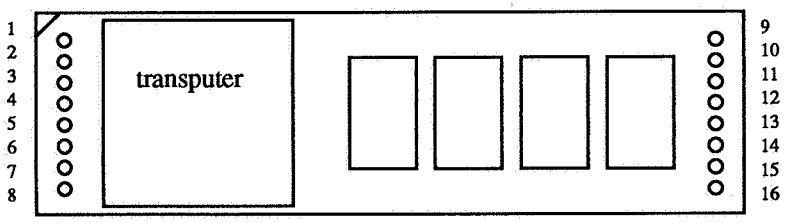
Introduction The Transtech TTM30 TRAM (TRAnsputer Module) is a small industry standard daughterboard for the Transtech range of TRAM motherboards. It has 256 KBytes of static RAM and an IMST801 transputer with a fast non multiplexed external memory interface giving 2 cycle memory access. It is ideal for transputer systems where memory bandwidth is a bottleneck.

TRAM Standard Measuring only 1.05" by 3.66" (2.67mm by 9.30mm) the TTM30 conforms to the published TRAM standard, allowing them to be plugged easily onto a wide range of motherboards for many different host machines. Up to 10 TRAMs can be accommodated on a Transtech TMB08 board for IBM PC XT or AT's and compatibles, 4 on the Transtech TMB04 and TMB05, 16 on a TMB12 double extended eurocard and 32 on the MCP1000 Multi Computing Platform for Sun workstations, allowing rapid prototyping of transputer systems. Transtech TRAMs are also compatible with motherboards from other manufacturers. Further details on the TRAM standard and TRAM Module Motherboard Architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

Transtech TTM30

Functional Description

TRAMs use 16 pins for communication with the motherboard and for obtaining power. However, TRAMs that are larger than size 1 have more than 16 pins, with the extra pins providing more power and ground connections. The extra pins also propagate the signals from the motherboard below to allow stacking of modules. The link speed of the TRAMs is selected by two pins. When both are held low the links operate at 10 Mbits/sec and when high at 20 Mbits/sec. This is implemented by jumpers or switches on the motherboards. The allocation of the pins are shown in the following diagram.



1 Link2Out	9 Link3In
2 Link2In	10 Link3Out
3 VCC	11 GND
4 Link1Out	12 Link0In
5 Link1In	13 Link0Out
6 LinkSpeedA	14 notError
7 LinkSpeedB	15 Reset
8 ClockIn(5MHz)	16 Analyse

Ordering Information

Part Number	Processor Type	Processor Cycle Time (ns)	Memory (KBytes)	Memory CycleTime (ns)
TTM30-20	IMST801-20	50	256	100
TTM30-25	IMST801-25	40	256	80
TTM30-30	IMST801-30	33	256	67

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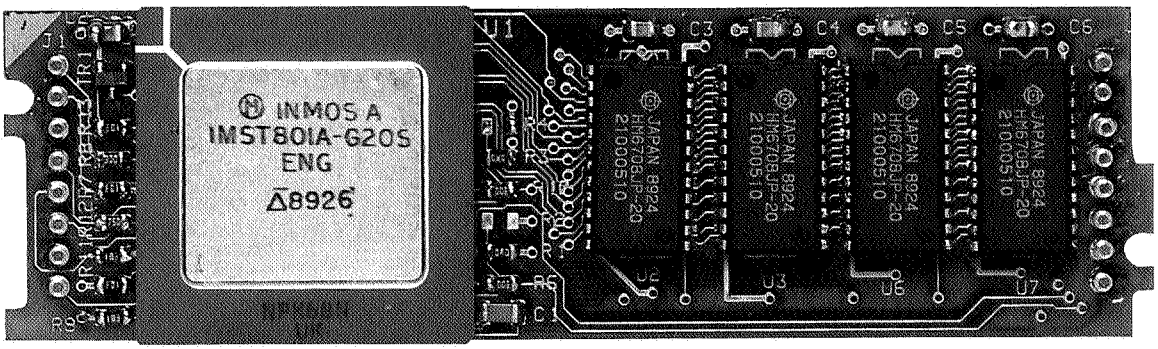
Document Reference:TTM30FLY1189

TTM High Performance T801 TRAM TTM
Transtech TTM31

Features

- **IMST801 running at 20, 25 or 30 MHz**
- **1 MByte fast static RAM**
- **Non multiplexed external memory interface**
- **2 processor cycle external memory access (minimum 67 ns)**
- **Four serial transputer links**
- **Only 16 active pins**
- **Industry standard size 1 TRAM**
- **Compatible with Transtech range of TRAM motherboards**



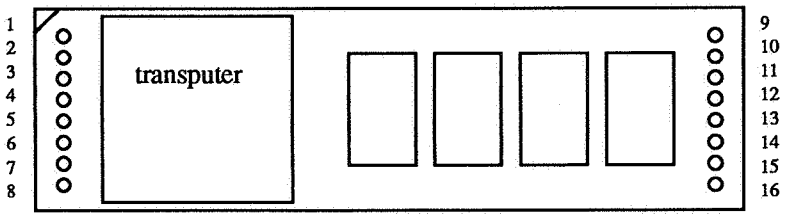
Introduction The Transtech TTM31 TRAM (TRAnsputer Module) is a small industry standard daughterboard for the Transtech range of TRAM motherboards. It has 1 MByte of static RAM and an IMST801 transputer with a fast non multiplexed external memory interface giving 2 cycle memory access. It is ideal for transputer systems where memory bandwidth is a bottleneck.

TRAM Standard Measuring only 1.05" by 3.66" (2.67mm by 9.30mm) the TTM31 conforms to the published TRAM standard, allowing them to be plugged easily onto a wide range of motherboards for many different host machines. Up to 10 TRAMs can be accommodated on a Transtech TMB08 board for IBM PC XT or AT's and compatibles, 4 on the Transtech TMB04 and TMB05, 16 on a TMB12 double extended eurocard and 32 on the MCP1000 Multi Computing Platform for Sun workstations, allowing rapid prototyping of transputer systems. Transtech TRAMs are also compatible with motherboards from other manufacturers. Further details on the TRAM standard and TRAM Module Motherboard Architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

Transtech TTM31

Functional Description

TRAMs use 16 pins for communication with the motherboard and for obtaining power. However, TRAMs that are larger than size 1 have more than 16 pins, with the extra pins providing more power and ground connections. The extra pins also propagate the signals from the motherboard below to allow stacking of modules. The link speed of the TRAMs is selected by two pins. When both are held low the links operate at 10 Mbits/sec and when high at 20 Mbits/sec. This is implemented by jumpers or switches on the motherboards. The allocation of the pins are shown in the following diagram.



1 Link2Out	9 Link3In
2 Link2In	10 Link3Out
3 VCC	11 GND
4 Link1Out	12 Link0In
5 Link1In	13 Link0Out
6 LinkSpeedA	14 notError
7 LinkSpeedB	15 Reset
8 ClockIn(5MHz)	16 Analyse

Ordering Information

Part Number	Processor Type	Processor Cycle Time (ns)	Memory (MBytes)	Memory CycleTime (ns)
TTM31-20	IMST801-20	50	1	100
TTM31-25	IMST801-25	40	1	80
TTM31-30	IMST801-30	33	1	67

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Document Reference:TTM31FLY1189

MCS

Multi-Computing Systems

MCP

System Portfolio

Multi-Computing Systems

Transtech Systems, a world leader in the development of multi-processing systems introduces its Portfolio of high performance Multi-Computing products, an integrated suite of software and hardware products designed specifically to cater for the increasingly computational intensive demands of applications within Industry, Science, and Commerce.

Computational performance reaching into the hundreds or even thousands of MFLOPS is delivered through the utilization of RISC based multiple processor technology and made possible by some of the most advanced operating system software now available for parallel processing machines.

The Systems are fully integrated in to the 'de-facto' standard host for computing engines, the Sun Workstation. The combination provides all the necessary support for developing new software as well as enhancing existing Sun resident applications.

There is no restriction to the range of applications that can benefit from this technology. The techniques used for parallel processing are surprisingly familiar for software developers and users of the more traditional (and restrictive) sequential machines.

Multi-Computing Platforms

The hardware products which deliver the Computational Performance to provide users with a sensible and flexible means of tailoring systems to meet specific requirements.

VME based Computing Platforms are provided for use with the Sun-3, Sun-4, and the VME based SPARCstations. The flagship of the series, the MCP1000, is a 4 user system capable of accommodating up to 32 RISC based processing units, currently equivalent to 60 MFLOPS. The MCP501, a smaller but equally flexible 2 user product supports up to 8 processing units and, additionally, makes an ideal interface to external equipment. The 386i is supported by two versatile AT bus products developed by Transtech Devices, accommodating up to 10 processing units.

The processing units are the fundamental building blocks of the system and the key to its flexibility. Implemented using the Industry Standard plug-in Transputer Module format, the computing elements are fitted to the Computing Platforms as daughter boards and configured, by software, to meet the customers specific requirements. A wide variety of processing elements are available ranging from basic but powerful computational nodes, with varying amounts of memory, through to application specific devices such as Graphics/Display Controllers and SCSI Interfaces.

Multi-Computing Software

The infrastructure which enables the tremendous potential for large multi-processor systems to be unleashed and applied to a diverse range of applications.

A variety of software products have been developed to harness this potential including the REMOTE Resource Management Toolkit, *GENESYS II*, an advanced Generic Operating System for Multi Processor Systems, and the TDS, a Transputer specific package for developing Occam software.

The REMOTE Resource Management Toolkit seamlessly integrates the various members of the Multi-Computing Platform family into their host Sun workstation environments. It is responsible for handling all aspects of resource management across the Sun network, and provides a generic interface to support cross portability of software between Computing Platforms.

The *GENESYS II* Operating System is an extremely powerful, yet efficient, software environment for developing portable parallel software with the minimum of fuss. It is capable of supporting all of the accepted parallel processing paradigms in the Computer Industry and the standard languages such as C and FORTRAN. *GENESYS* enables users to focus on the application rather than on the underlying hardware infrastructure. All the necessary tools for parallel software development are provided, extending from simulation facilities through to full concurrent symbolic debugging support.

For further information on any of these products please contact Transtech Systems or your local Transtech distributor.

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TSS

Transtech Software Overview

TSS

FOR IBM PC PLUG IN TRANSPUTER BOARDS

Introduction

Transtech support various programming systems for their IBM PC plug in transputer boards. The most popular are the Occam based TDS (Transputer Development System) and Toolkit, and the 3L scientific language compilers for C, FORTRAN and Pascal.

3L's scientific language compilers allow programs written in standard C, FORTRAN or Pascal to be quickly and easily ported to run on Transtech's transputer boards, providing access to a very high performance powerful workstation in a PC. With slightly more effort programs can be extended to run on multiple transputer arrays.

TSS-PLC Parallel C

- **Multi threaded tasks synchronised by either transputer channels or semaphores**
- **Access to the transputer's channel I/O and timer functions**
- **In-line transputer assembly language with access to C variables**
- **Microsoft C compatible DOS interface functions (int86, bdos etc.)**
- **31-character identifiers**

The C compiler implements the full K & R C language with many extensions

TSS-PLF Parallel FORTRAN

- **Multi threaded tasks synchronised by either transputer channels or semaphores**
- **Access to the transputer's channel I/O and timer functions**
- **Routines to provide access to MS.DOS functions and facilities of the host PC**
- **IMPLICIT NONE**
- **DO WHILE construct**
- **INCLUDE statement**
- **Bit handling intrinsic functions**
- **Data initialisation in type statements**
- **Extended range of DO loops**
- **Lower case in program text**
- **31-character identifiers**

The FORTRAN compiler is a full implementation for the transputer of the FORTRAN 77 language as defined by the ANSI standard X3.9-1978.

TSS-PLP Parallel Pascal

- **Multi threaded tasks synchronised by either transputer channels or semaphores**
- **Access to the transputer's channel I/O and timer functions**
- **Routines to provide access to MS.DOS functions and facilities of the host PC**
- **Modules for separate compilation: IMPORT and EXPORT**
- **Source file INCLUDE**
- **32-bit and 64-bit REAL data types**
- **Low level facilities: in-line transputer assembly language with access to Pascal variables, ADDRESS function, bit-vector operators, UNIV parameter type**

The Pascal compiler is a full ISO conforming implementation of Pascal for the transputer.

TSS

Transtech Software Overview

TSS

FOR IBM PC PLUG IN TRANSPUTER BOARDS

TSS-TDS (D700D) Transputer Development System

- ♦Integrated 'folding editor' user interface
- ♦Memory resident program development tools
- ♦Help key, tutorial file and many introductory examples
- ♦Full implementation of Occam 2 language
- ♦Optional machine code embedded within Occam
- ♦Automatic recompilation of program components
- ♦Mathematical and input/output libraries
- ♦Easy evolution from host development to target system
- ♦Source level debugging tool
- ♦Tools for creating multi processor programs in EPROM
- ♦Targets mixed network of transputers

The TSS-TDS (D700D) provides a fully integrated Occam 2 development which runs on a transputer board plugged into a PC. A server program runs on the PC providing terminal and file input/output support. The user interface is the 'folding editor' which is initialised when the system is booted.

TSS-TST (D705B) Occam Toolset

- ♦Occam 2 development system
- ♦Targets mixed network of transputers
- ♦Support for machine code inserts
- ♦Support for mixed language developments
- ♦Tools to aid system building and ensure program consistancy
- ♦Source level debugging tools
- ♦Support for teams of developers
- ♦Easily used with project management and source control utilities

The TSS-TST (D705B) provides a complete Occam 2 system with development tools which run on a transputer board plugged into a PC. A server program runs on the PC providing terminal and file input/output support. The development tools are run from the DOS command line.

Other Software

Transtech can also supply the GENESYS, Helios and Trans-IDRIS operating systems as well as the 3L ROM configurer.

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Document Reference:TSSFLY0889

MCP

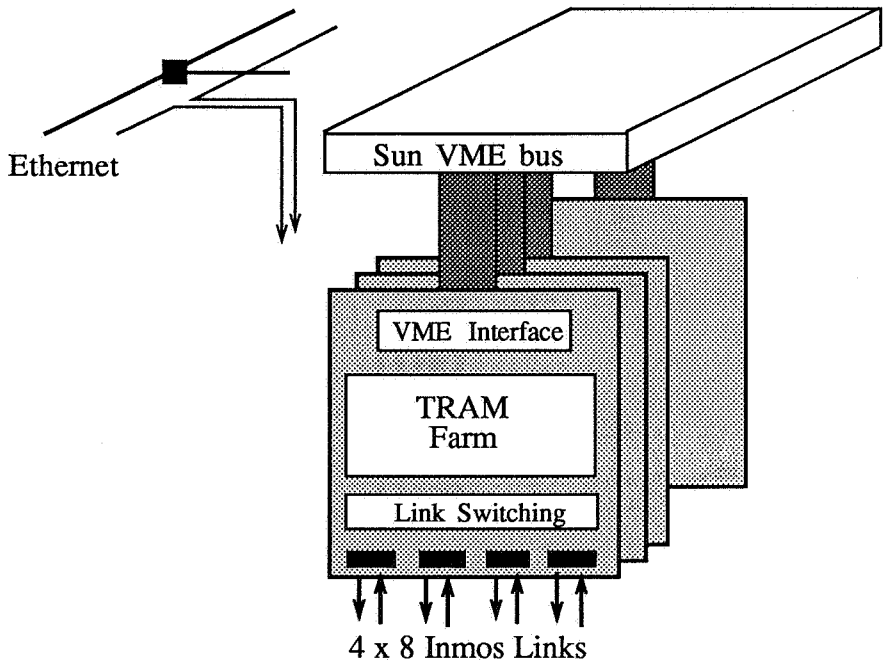
Multi-Computing Platform

MCP

MCP1000-3

Features

- **Transputer Computing Platform for Sun Workstations, capable of accommodating up to 32 Industry Standard TRAMS.**
- **A high performance VME interface enabling up to 4 users to utilize each computing platform from any point on a Sun Network.**
- **Fully integrated into SunOS Unix and NFS, providing access to the most advanced Software Environments for Transputers.**
- **An OPEN system architecture, capable of communicating and working with other Transputer Systems and Custom Hardware.**



Description

The MCP1000-3 Computing Platform has been designed to plug directly into the standard 9U VME slots of **Sun-3** and **Sun-4 Workstations**, providing access to the unrivalled flexibility and computational performance of multiple and parallel processor technology.

Each Computing Platform is capable of supporting up to **32 Industry Standard Transputer Modules (TRAMS),** thus providing a maximum computational capability of **60 MFLOPS** per Platform, and the choice to select processing elements with amounts of memory ranging from 16k bytes to 26 Mbytes each. Up to 4 independent users can access and share the Platforms resources from any point on the Sun network: access from PCs, VAXs, and VT100 terminals via the Sun network is also supported.

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Multiple Platforms can be configured to run within the same Sun Workstation, as large multi-user computational engines, or across the Sun Network, as a distributed Computing Facility.

A comprehensive range of **leading edge software** packages and developement environments is available enabling users to utilize the resource as a development platform, educational facility, or as a turn-key system.

MCP

MCP

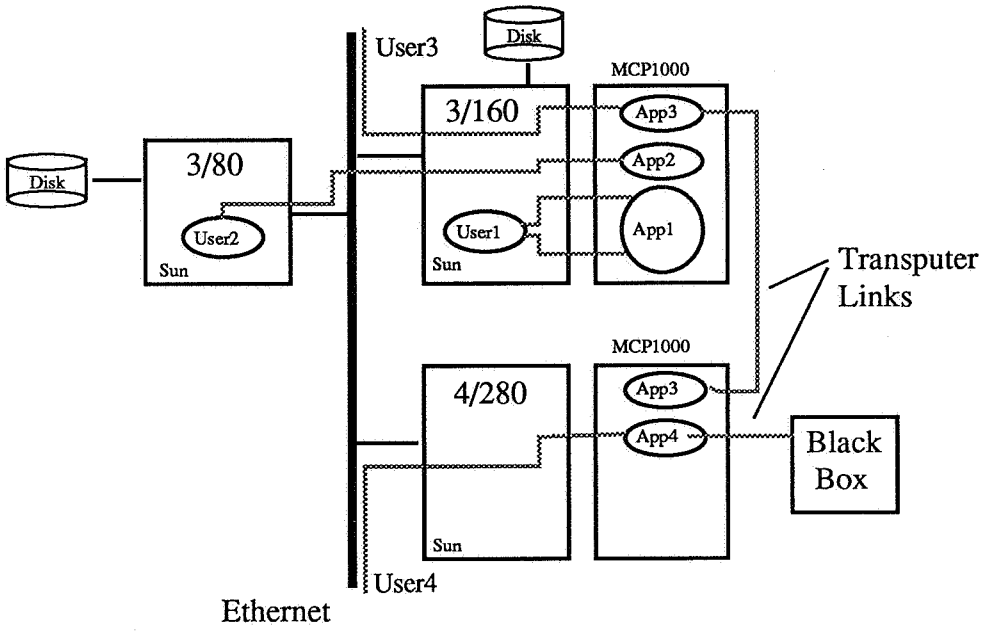
MCP1000-3

Open System

The Computing Platform adopts an open architecture and can also be used as a **high bandwidth Sun/VME bridge**, providing multi-user and networked access to other Transputer products and custom-hardware. This is a **cost effective** technique for increasing the accessibility of existing Transputer based resources.

Networking

When installed within a Sun-3 or Sun-4 Workstation, the MCP1000 Computing Platform(s) is represented as a suite of easily controlled SunOS Unix resources. A layer of System Software is then provided to enable users, from anywhere on the Sun network, to access these resources and utilize them with their chosen Development Environments and/or Software Packages.



Why Transtech?

Transtech Systems Ltd. is a **Unix house** which is totally committed to developing and supporting leading edge Transputer products for Unix based Operating Systems and associated Workstations.

We support **more Transputer users with Sun Workstations than any other company** and pride ourselves on having the most mature and wide-ranging portfolio of Unix based software and hardware products in this arena.

Transtech protects the investment made by its customers by adopting an **open system philosophy** and adhering to **Industry Standards** whenever appropriate. We never forget that our **customers have a choice** and that they may need to retain portability between our Systems and those of other companies.

The MCP1000-3 Computing Platform is just one example of the Quality Products available from Transtech Systems. Its reliability, flexibility and performance is unrivalled and has become the benchmark from which other companies design their latest products. Information is also available on other products associated with the MCP1000 and can be obtained by contacting Transtech directly or through your local Transtech distributor.

ts10010689

MCP

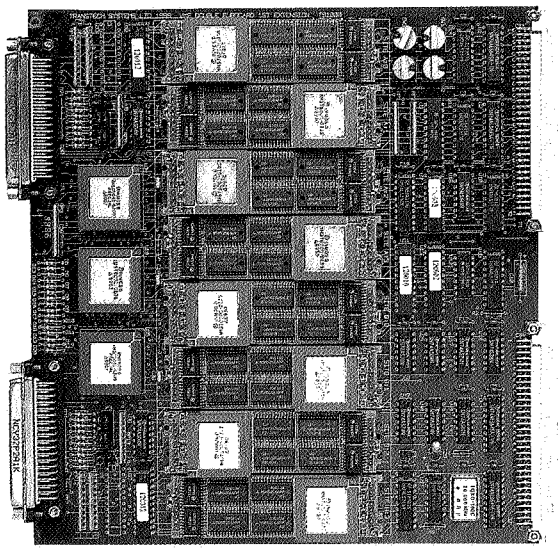
Multi-Computing Platform

MCP

MCP501

Features

- **Transputer Computing Platform capable of accommodating up to 8 Industry Standard TRAMS.**
- **Incorporates a high performance multi-user VME interface.**
- **Compatible with other Multi-Computing Platforms from Transtech**
- **Can be fully integrated into SunOS Unix and NFS, providing access to the most advanced Software Environments for Transputers.**
- **An OPEN system architecture, capable of communicating and working with other Transputer Systems and Custom Hardware.**



Description

The MCP501 Computing Platform has been designed for use in VME based computer systems ranging from small high performance embedded systems through to professional development environments incorporating Sun-3 and Sun-4 workstations.

Each Computing Platform is capable of supporting up to **8 Industry Standard Transputer Modules (TRAMS),** thus providing a maximum computational capability of **15 MFLOPS** per Platform. **Multiple Platforms** can be configured to extend computational capability and/or functionality. The consistent and scalable architecture also enables different Computing Platforms to be integrated into the same VME bus environment, running the same applications software.

The Open Systems approach of the standard Module Motherboard approach provides users with an almost infinite degree of flexibility to configure the systems to meet their specific requirements. A wide range of modules are available ranging from the basic computational elements (with varying amounts of local memory) through to the recent Application Specific products which range from Real Time Graphics and Display Controllers through to Industry Standard interfaces such as RS232 and SCSI.

A comprehensive range of **leading edge software** packages and development environments is available enabling users to utilize the resource as a development platform, educational facility, or as a turn-key system.

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MCP

MCP

MCP501

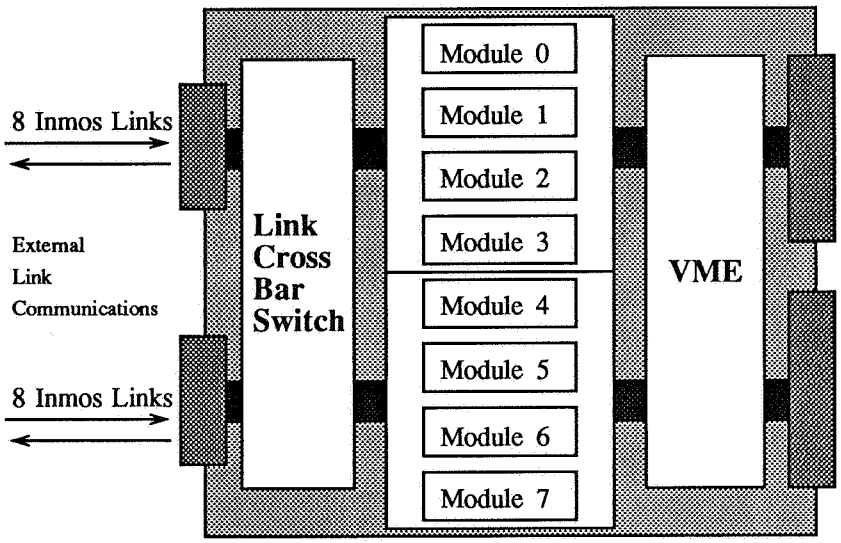
Open System

The Computing Platform adopts an open architecture and can also be used as a high bandwidth Sun/VME bridge, providing multi-user and networked access to other Transputer products and custom-hardware. This is a cost effective technique for increasing the accessibility of existing Transputer based resources.

System Architecture

The MCP501 is an extended Double Eurocard VME system motherboard capable of accommodating up to 8 Industry Standard Transputer Modules together with a range of i/o facilities. An intelligent high speed 32-bit multi-port controller and two medium speed ports are made available to exploit the high performance 32-bit VME bus.

The 8 plug-in TRAM module slots are arranged as two 'sites', each of which, if required, can be controlled and utilized independently. The user has complete freedom to connect any module conforming to the Industry Standard, ranging from the small size 1 width (single slot) variety through to size 8. A software controlled Link Cross-Bar Switch supports complete reconfigurability, enabling users to select the most desirable processor topology. The Cross-Bar switch also enables any 8 Transputer Links, together with the usual sub-system services, to be taken to each of the two 37-way D-Type connectors, providing a means of connecting to other Multi-Computing Platforms and Transputer hardware.



Software

Users of the Computing Platform have access to a rich variety of supporting ***MCS*** software products ranging from Standard Compilers and development environments through to high level Operating Systems.

The **REMoTE** REsource Management Toolkit seamlessly integrates the board into Sun3 and Sun4 workstation environments, handling all aspects of resource management across a Sun network, and provides an ***MCP*** generic interface which is utilized by the other ***MCS*** software products.

Integration into other VME systems (which are Rev B and C.1 compliant) is also supported. Users wanting migrate software developed on any of the Sun hosted Computing Platforms or to develop new stand-alone systems can access comprehensive documentation describing the VME interface and associated software. Transtech are pleased to advise customers interested in developing their own systems and is capable of offering a full software consultancy service. Further information can be obtained direct from Transtech.

MCS

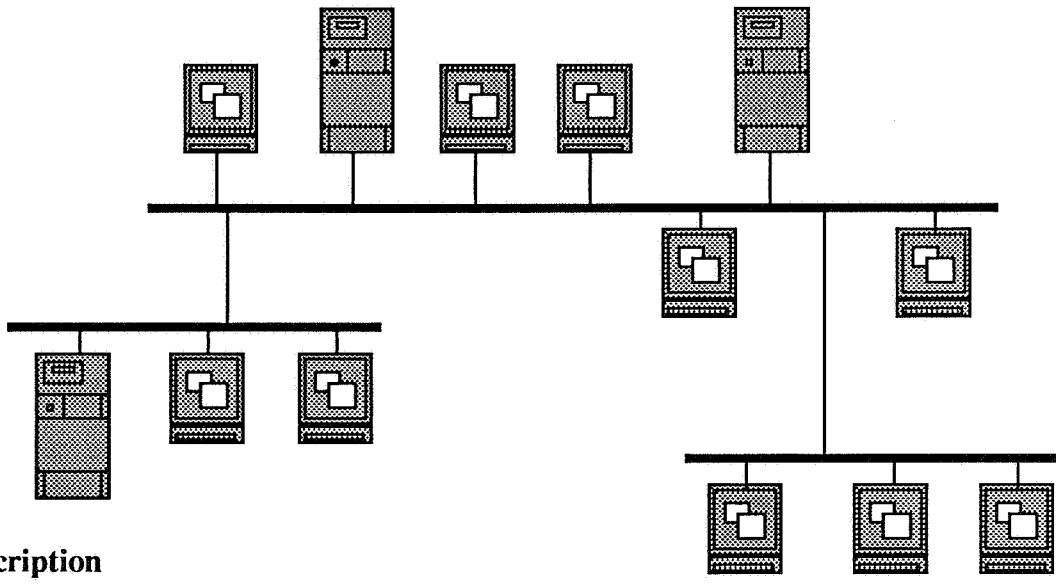
Multi-Computing Software

MCS

REMoTE (REsource Management Toolkit)

Features

- **Resource Management Software Toolkit for Computing Platforms**
- **Enables one or a number of Computing Platforms to be integrated into a network of Sun Workstations, providing users with a consistent, uncluttered model of the Computing Resources**
- **Provides a consistent interface across the entire range of Computing Platforms**
- **State of the art Resource Search and Acquisition capabilities which can support customer defined hardware extensions and complex networking**
- **Provides a comprehensive suite of Resource Monitoring, Interrogation, and Diagnostic utilities.**



Description

Sun Workstations are recognized as the leading Unix based vehicle for supporting Transputer based Development and Turn-Key Systems. Transputer users are now able to realize the full potential of Unix in Multiple User and Workstation environments.

The REMoTE Resource Management Toolkit is the only system which fully utilizes this potential to provide a coherent network wide management system for the control and utilization of distributed Computing Resources, thus bypassing the more primitive and frequently inappropriate approach of having to physically *rlogin* across networks of Sun workstations

REMoTE enables users, from anywhere on the network, to interrogate, acquire, and utilize the Computing Platform(s) resources. Each computing platform, regardless of type, is provided with a standard interface so that users need only concern themselves with the computational capabilities required. REMoTE is ideally suited for the management of resources in large multi-user educational and development environments.

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MCS

MCS

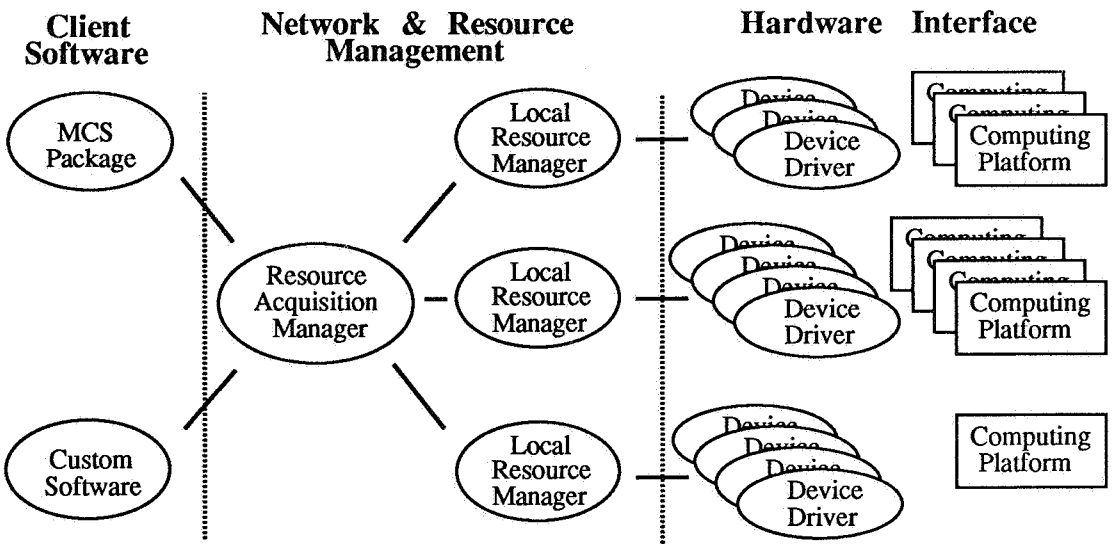
REMoTE

Hardware Interface Standard

At the lowest level, REMoTE provides the user with a suite of Unix device drivers, capable of driving and communicating with any member of the Computing Platform product family. A consistent and standard interface is utilized by each device driver so that application software can interact with any member in the Product Family without having to be concerned with issues of compatibility. As far as the user is concerned, each device driver implements the same *open, close, read, write, ioctl,* and *select* system calls. As a result, users can develop software on one Platform without losing the ability to utilize the other Platforms which offer a different mix of communication performance, multi-user and computational capability, and cost. Most users, however, do not need to concern themselves with these details as device interfacing it is already integrated, transparently, into all ***MCS*** products.

Networking

The Network and Resource Management System works at a higher level of abstraction, taking full responsibility for the interrogation, selection, and utilization of each Computing Platform on the network. The interrogation facility enables a user to determine the type, availability, and usage of resources currently installed. Selection can then be achieved by passing to the Management System details of the resource required and, if the user wishes, a description of the machines that are likely to contain it. This later capability is only an option as the system is entirely capable of locating and allocating all resources on the network.



An additional layer of functionality beyond the basic Networking Model is provided by REMoTE, which enables users to cater for dedicated computational resources and custom hardware. Each Computing Platform can be described using a set of user definable Dedicated Resource Identifiers. Using these Identifiers a user can describe, more concisely, the type of Computational Resource that is required to support a particular activity.

REMoTE provides users with an ideal mechanism for distinguishing between different types of resource within a network. The user is not concerned so much with the location, only the main features of the resource. Other resources provided by REMoTE include a comprehensive suite of diagnostics, configuration, and resource monitoring utilities which further facilitate the integration and management of Computing Platforms.

If you would like further information on REMoTE or any other ***MCS*** product please do not hesitate to contact your local Transtech Office.

MCS

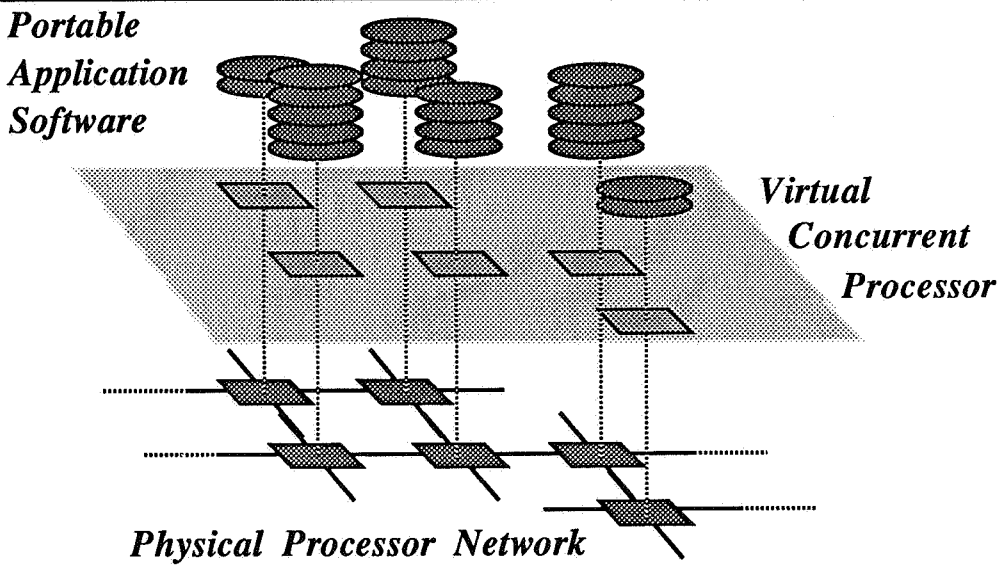
Multi-Computing Software

MCS

GENESYS II

Features

- **An Operating System for Parallel and Multi-Processor Architectures.**
- **Provides all the necessary services for developing large, complex, and portable parallel processing applications.**
- **An Open System which Enables users to track advances in hardware technology without sacrificing existing investments in Software.**
- **Intimately integrated with SunOS Unix enabling the full power of a Sun Workstation to be exploited and complemented by the Transtech Multi-Computing Platform.**



Description

GENESYS is a GENEric Operating SYStem designed specifically to meet the requirements of multi-processor systems and the needs of the expanding range of applications which now seek to take advantage of this powerful and flexible technology. Currently implemented on the Transputer, Sun-3, and Sun-4 workstations, *GENESYS* provides the applications developer with a flexible and consistent interface which allows for the maximum utilization of existing software, together with the ability to benefit from the more advanced processors which are now becoming available.

Designed initially for use with large Massively Parallel Computers in the United States and Europe, the Operating System provides a rich suite of resources and many of the accepted standards now used in the parallel processing industry. The developer has access to standard languages, such as C and FORTRAN, and can choose from a number of common parallel processing and message passing paradigms. By avoiding the more obscure and proprietary design principles, *GENESYS* steers software development in the direction of the application, enabling users to gain maximum insight in exploiting parallelism rather than catering for the idiosyncrasies of the underlying hardware.

Seamlessly integrated with the Sun Workstation, incorporating SunOS Unix, SunView and the SunPro development environment, GENESYS also provides users with a familiar professional environment for development (standard languages, symbolic debuggers etc.) and the freedom to utilize existing investments in software, design procedures, and experience.

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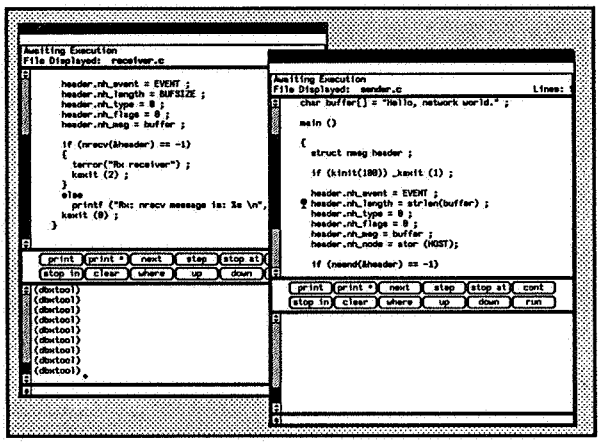
MCS

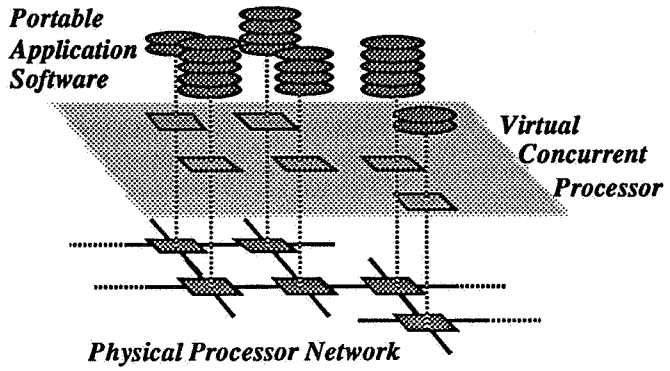
Multi-Computing Software

MCS

Debugging Software with GENESYS

- **Full Source Level Symbolic Debugging with *GENESYS* and Trollius based Operating Systems.**
- **Debugging support for complex parallel software, operating across any number of processors ... including the host Sun workstation.**
- **Integration within existing Sun resources for a consistent software development strategy.**





Transtech has developed the first full source level symbolic debugging system for *GENESYS* and other Operating Systems incorporating its C and FORTRAN compilers. The facility provides all the standard functions associated with symbolic debugging, enabling software programmers to apply these standard techniques to the development of parallel software for execution across the increasing range of processors supported by *GENESYS*.

The symbolic debugging capability extends across all processing devices, including the host Sun workstation(s), processors on the Multi-Computing Platforms, and any external hardware supporting *GENESYS*. Software executing on the host Sun workstation can take advantage of Suns own '*dbxtool*'. Software executing on the Multi Computing Platform or any external hardware uses a computable version offering the same functionality.

The symbolic debugger enables a programmer to monitor and trace the execution of a program executing within the *GENESYS* Operating System. Multiple debuggers can be used to trace several programs simultaneously and monitor data being transferred between them.

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MCS

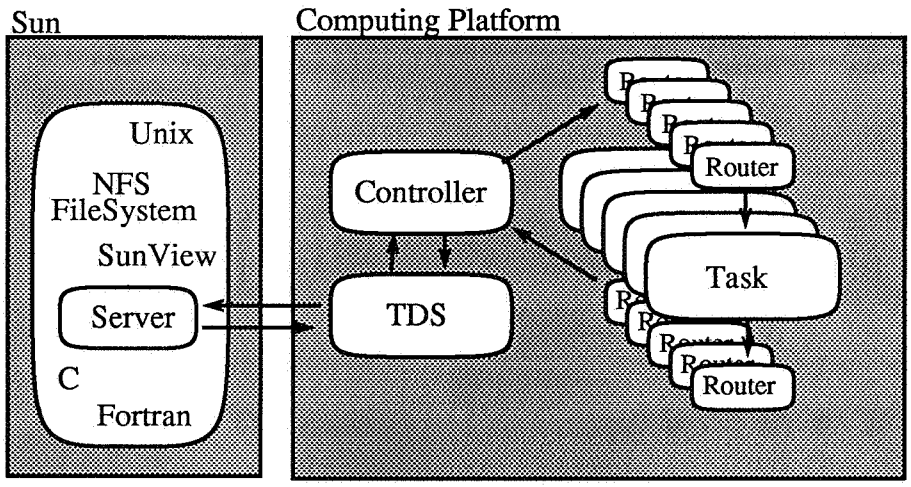
Multi-Computing Software

MCS

TDS

Features

- **Software Developement Environment for Transputers**
- **Conformant & Cross Compatible with the Inmos D700 TDS**
- **Full Implementation of Occam2 programming language**
- **Access to SunOS Unix filestore across Sun NFS**
- **Multi-user networked resource**
- **Supported across all Computing Platforms**



Applications

- Development of single-processor and multi-processor embedded systems
- Development of Sun accelerator software for Computing Platforms
- Sun-based evaluation of concurrent programming and Transputers

Description

The IMS D700 Transputer Development System (TDS) was developed by Inmos to run on the IBM-PC, under MSDOS, and to provide a complete occam programming system for the Transputer. The TDS is a self contained environment where occam programs can be edited, compiled, configured, run, and debugged, all on the Transputer.

Transtech Systems offer a fully compatible version of the TDS, which runs on all Computing Platforms, and gives TDS users access to many of the features provided by the Sun Workstation.

The enhanced version of TDS can be used in a single workstation, as a dedicated resource, or as is more frequently the case, within a network of Suns and made available to its users as a network-wide computing facility. Multiple user capability enables the TDS to be used within environments ranging from large software development projects through to educational facilities.

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MCS

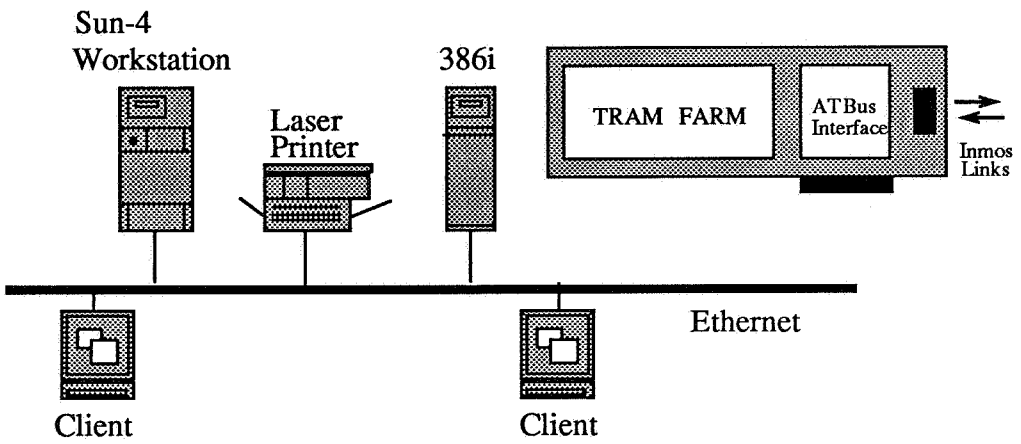
Multi-Computing Systems

MCP

Transputer Solutions for Sun 386i

Features

- **Control and Utilization of AT bus Transputer boards as Unix resources.**
- **Two Transputer boards can be installed in each 386i, providing up to two independent users with access to their resources.**
- **Fully integrated into the Sun network, enabling users to utilize the Transputer boards from any other Sun workstation.**
- **Access to the comprehensive range of Unix based Multi Computing Software (MCS) products from Transtech Systems.**



Description

Sun Microsystems boasts the widest ranging and most highly respected family of Workstation products now available. Their approach towards distributed computing, having established the phrase **The Network Is The Computer**™, is unrivalled to the extent that a large proportion of the Computer Industry now looks to Sun as a major driving force behind Open System Standards.

As one of the most recent additions to their product family, the 386i extends the availability of Sun Microsystems technology to the Personal Computer Market. Each Sun 386i, while providing the most easy-to-use version of the UNIX Operating System , SunOS, also enables users to access the ubiquitos DOS operating system and utilize AT Bus expansion ports.

Realizing this potential, Transtech Systems is the first company to develope a range of products based around the exelent SunOS UNIX Operating system and the versatile AT Bus Transputer products from Transtech Devices. The advantages are significant:

Transtech Devices produces two AT bus Transputer boards which are supported by Transtech Systems for the Sun 386i workstation, the TMB04 and the TMB08. Each of these boards are reconfigurable, can support DMA communication across the Sun hosted AT Bus, utilize Industry Standard Transputer Modules (TRAMS) and are capable of connecting to additional Transputer equipment.

By utilizing these products as Unix hosted resources, the user gains access to the many excellent **leading edge software** products and devlopment tools now available from Transtech for use with the other members of the Computing Platform family.

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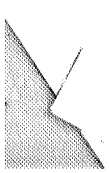


GENESYS: An Operating System for Parallel Computers

Paul Hudson, Stephen Bradshaw

Transtech Technical Note, No. 2.
June 1990.

TRANSTECH

parallel
technology

Acknowledgement

GENESYS is a commercial Operating System for distributed memory parallel processing systems. It is based on the Trollius Operating System for transputers originally developed at Cornell and Ohio State Universities. Transtech acknowledges the development efforts of these Universities to create Trollius, and is grateful for the assistance received when developing GENESYS.

Company Profile

Transtech was formed in March 1986 as the research, government establishment and education agent for INMOS transputer based products. The portfolio was quickly expanded to include systems from the key parallel processing start-ups. Commitment to customer support and service, backed by an expert technical team, has driven Transtech's growth and it is now recognised as the world's leading transputer supplier. Already a major manufacturer, Transtech has led the development of open systems for both parallel processing hardware and software; this proven on a growing family of host enviroments.

Transtech has built dedicated sales and customer service teams, these being experienced people in both the commercial and technical requirements of supporting high performance systems. Combining these skills with a well developed contact and information database has given much to Transtech's reputation for satisfying customer demand. Transtech is used to supporting OEM and VAR customers as well as end users.

Transtech supports the most comprehensive range of transputer systems, focusing on high performance and superior functionality at sensible cost. In particular, Transtech has led the marketplace in transputer module and motherboard development. Transtech now boasts three extensive ranges of transputer module products: generic, high performance, and application specific. Motherboards are available for PC, PS/2, VME, Sun, Apollo, Macintosh and stand-alone systems. Transtech also boasts the worlds largest installed base of Sun hosted transputer systems, complemented with its own high performance compilers and Operating System GENESYS.

1 Introduction

GENESYS is an interactive development environment for distributed memory, parallel processing systems. It delivers a range of services which enable application software developers to utilize the "hardware" in parallel systems in a straightforward manner. These range from network-wide/network-transparent services (at the lower levels) to a number of programmer support tools such as symbolic debuggers.

The "hardware" model (see Figure 1) is based on the concept of a number (array) of compute nodes which are utilized in conjunction with a host node. Together, the array of compute nodes deliver the computational performance of the system. Currently, each compute node consists of a transputer (32 bits), an i860 processor (64 bits), or both, an amount of local memory (e.g. 4, 8, or 16 MBytes), and a communication interface; application specific interfaces are also supported. The compute nodes can communicate with each other and the host node to enable co-operative execution of related tasks and to transfer and distribute data across the parallel environment.

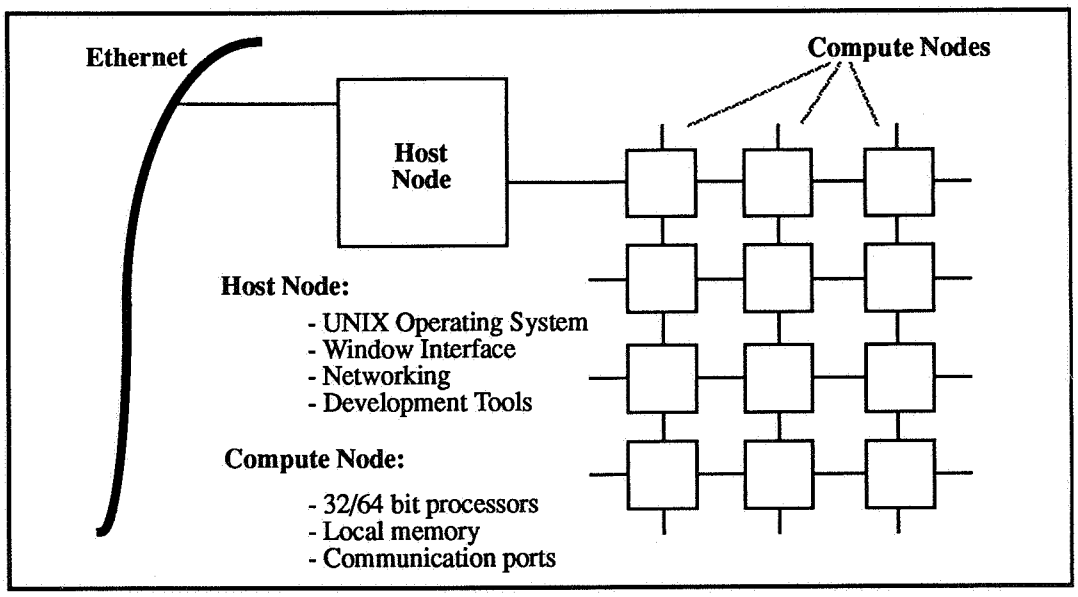
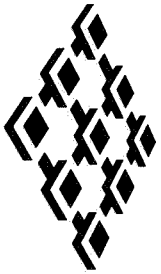


Figure 1 Model of system supported by *GENESYS*

The role of *GENESYS* is to present the "hardware" in a fashion which can be easily and efficiently exploited. Each compute node is booted with a suite of run-time services which are responsible for supporting applications running on that node. The services provided include:

- A "software" interface to communication hardware
- Dynamic process management
- Access to file systems on other nodes
- Support for ANSI FORTRAN and C



Some of the run-time services provided are utilized as transparent network wide resources such as network wide communication and access to remote file systems; applications do not have to be concerned with routing information across complex topologies. Only those services which are necessary for a parallel application need be used. An event driven strategy towards implementation is also used, thereby eliminating overheads traditionally associated with heavy weight Operating Systems.

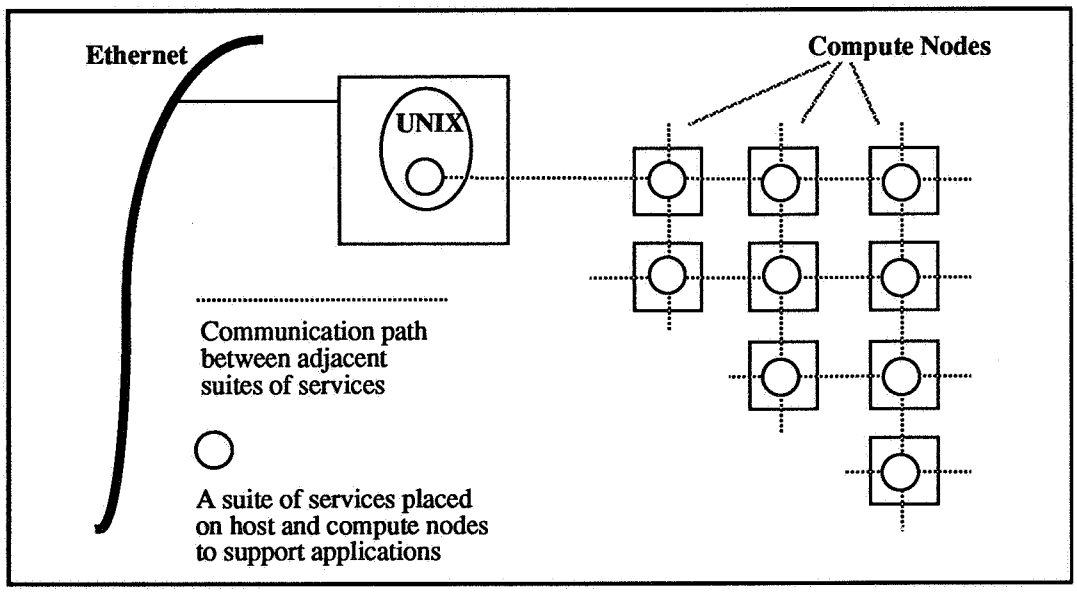


Figure 2 Run-time services are made available on each node to support applications

GENESYS is capable of booting across any connection topology which allows indirect communication between any two nodes. Services which cannot be delivered via direct hardware connection will be delivered indirectly.

Typically, the host node is a Sun workstation running UNIX, and the compute nodes are modules containing transputers, i860 processors, or both (see Reference [1]). Transputer links are used for communication between compute nodes, while communication between host and compute nodes relies on the use of the host interface bus (typically VME). Compute nodes can include additional application specific capabilities such as video display controllers, framegrabbers or disk controllers. *GENESYS* can also support many other types of processor and forms of inter-processor communication.

This Technical Note introduces the programming model adopted by *GENESYS* and then describes in more detail the services it provides. Additional information can be obtained from the documents described in the Bibliography.

2 The Programming Model of *GENESYS*

In its simplest form, a *GENESYS* based parallel system is one which consists of a number of host and compute nodes, each of which is capable of executing one or a number of sequential processes (or programs). These processes are written in standard ANSI FORTRAN or C, or both, and utilize a number of communication routines, supplied by *GENESYS* as library calls.

All nodes are considered to be capable of executing processes. Communication, whether it is between processes executing on the same or different nodes, takes the form of explicit data transfers. A sending process will identify a portion of data to be sent. The recipient will assign the received data to a specific region of memory or data structure.

2.1 Alternative Approaches

Applications developed with *GENESYS* can adopt a number of approaches towards the utilization of parallel hardware. This can range from existing sequential code running on individual nodes to more involved approaches which depend on the co-operative execution of a number of processes running on different nodes; execution of processes being possible on the host node, compute nodes, or both.

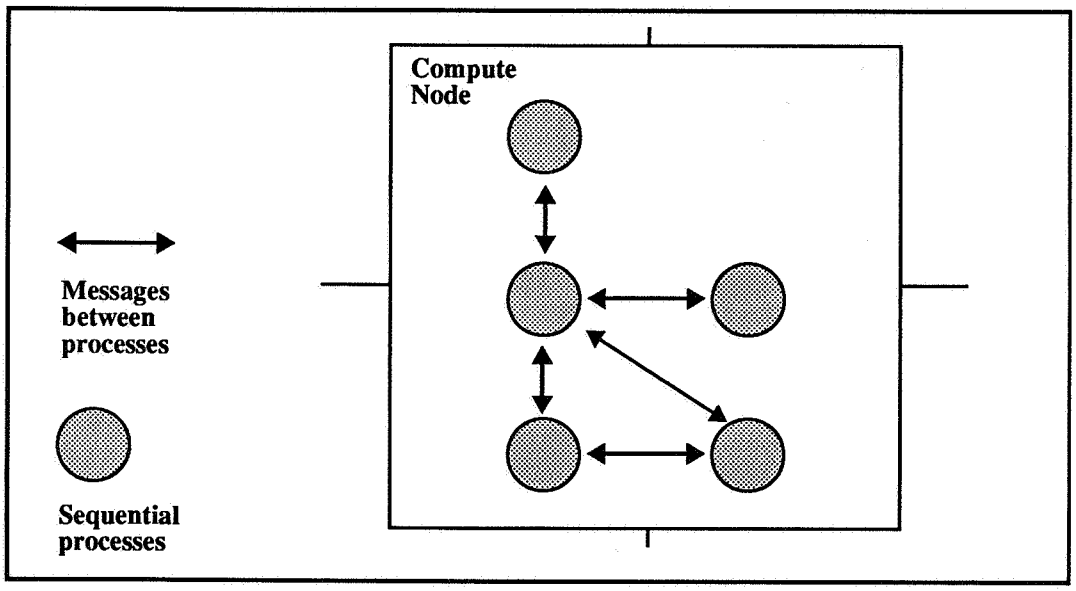


Figure 3 Communication of sequential processes on a single node

Concurrent implementations can adopt many of the approaches used for parallel design ranging from "domain decomposition", the partitioning of data and distributing it between an array of identical processes, to "functional parallelism" which involves piping the same data through a number of different processes.

2.2 Utilization of Host Node

The design of *GENESYS* acknowledges that some facilities are better provided by the Operating System of the host node (see Figure 4). Parallel applications generally do not operate in isolation, requiring access to high level user interfaces, networking capability, and support from other hardware or software sub-systems. From the software engineer's point of view, it is possible to utilize the best of both the UNIX and *GENESYS* worlds; using the established and familiar development environment of the host to ease the production of parallel applications and the powerful facilities of *GENESYS* to use the hardware to the full. In particular a number of complimentary products such as software design/management systems and visualisation packages will enhance the capabilities of the parallel system.

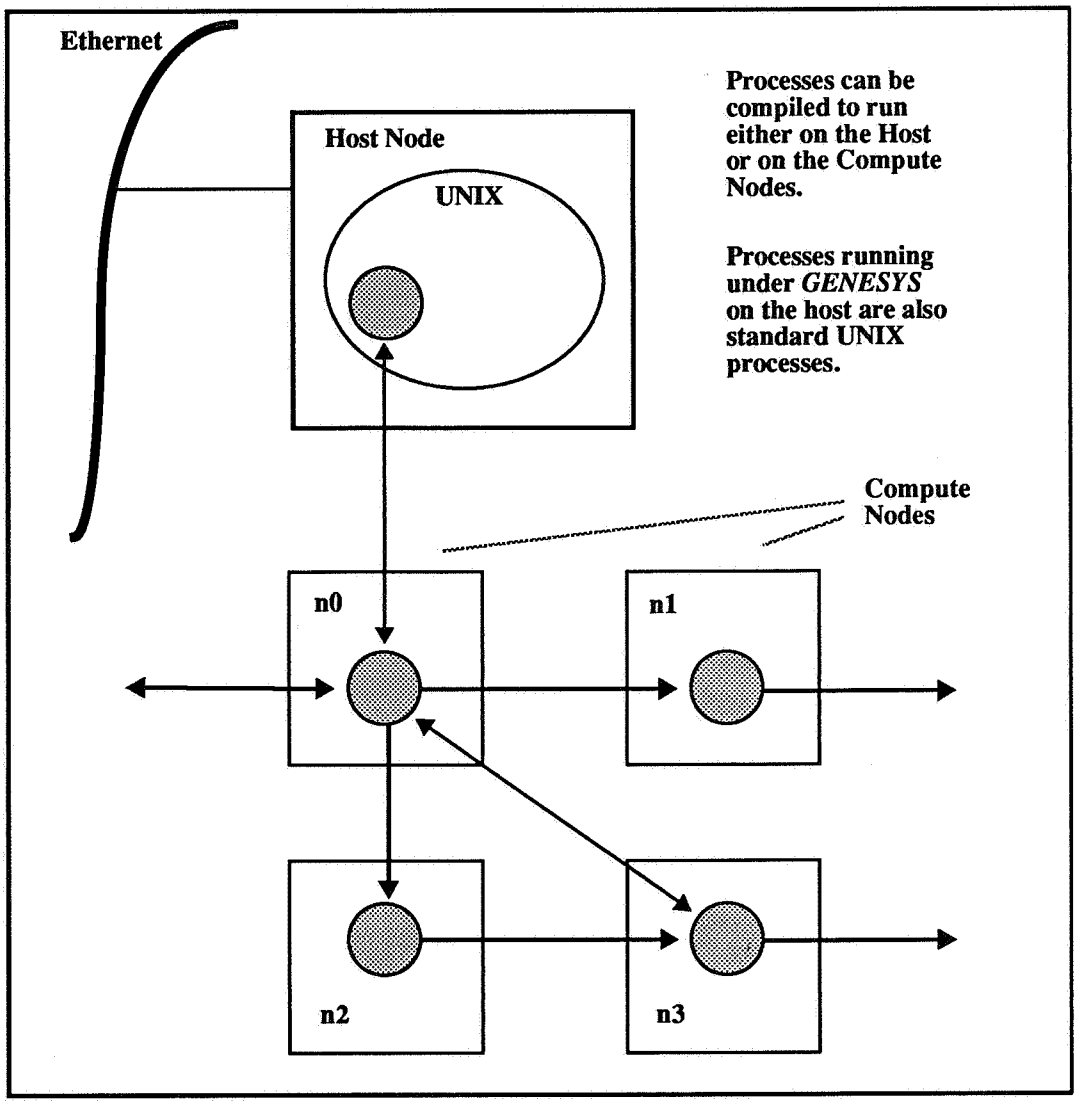


Figure 4 Communication of sequential processes between different nodes

3 Basic Services

Every process executing under *GENESYS* normally has access to the whole range of services provided, including inter process message passing, dynamic process management, and file system access. Users can choose which services should be supplied to each node, and thus obtain the exact configuration which best suits the application.

3.1 Message based Communication

Messages are the glue between the (sequential) building blocks of a parallel application. The parts of a parallel application communicate with one another by exchanging messages. The message facilities of *GENESYS* operate in the same way on the different hardware platforms, easing the problems of porting software. *GENESYS*, itself a parallel program, uses messages to implement services such as the file system interface.

A *GENESYS* process can send a message to any other process on any node or group of nodes. The body of the message is just a sequence of bytes - the interpretation is left to the sending and receiving processes.

Different nodes may have different hardware data representations. *GENESYS* provides for conversion of common data types as required. The conversion can be done explicitly by the program - necessary for complicated types - or implicitly as part of the process of sending the message.

Specifying the recipient of a message

The recipient process of a message is not identified directly. Instead, a receiving process indicates its willingness to accept messages of a certain *event* and *type*. A message's event and type are specified by the sending process. The events specified by the sender and receiver must be the same, while the types provide a filter to control message receipt.

Different levels of message passing

Most message passing in *GENESYS* programs uses either the *transport* (synchronous) or *network* level (asynchronous) functions. These permit messages of any length to be passed between any two nodes, with the route taken determined automatically. *GENESYS* also provides functions to pass messages between processes on the same node (*kernel level*) and between directly connected nodes (*datalink level*).

Messages do not go missing

Whatever level of message passing is used, all messages are either delivered, or buffered by *GENESYS* to await delivery. *GENESYS* never discards messages, unless explicitly requested to do so by the user.

Virtual Circuits

If several messages with the same event are to be sent in quick succession to the same process, a *virtual circuit* can be used to improve efficiency, where the route established by the first message is maintained for use by subsequent messages along the circuit. Each process can have up to 16 virtual circuits simultaneously active.While a virtual circuit is in operation no other process can use any links used by the virtual circuit.

Message buffering

By default, messages sent using the datalink or network level functions are buffered if they cannot be immediately delivered or forwarded. This permits the sender to continue execution without waiting for the receiving process. A message could potentially be buffered by every node though which it passes, but typically messages are either delivered without any need for buffering, or are buffered just on the node of the receiving process.

The buffering scheme guarantees that several messages of the same event and type sent from one process to another will arrive in the order that they were sent.

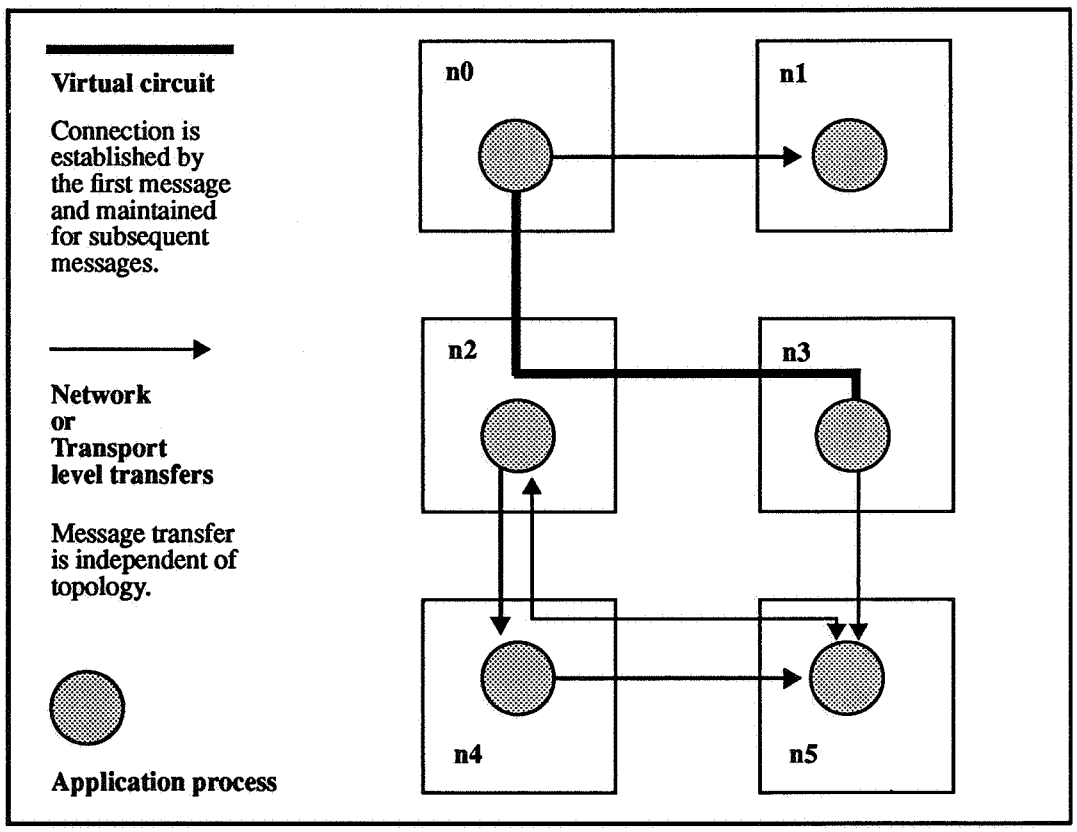


Figure 5 Network and Transport level services

Broadcast Services

In addition to point-to-point message transfer, *GENESYS* also enables messages to be distributed to and collected from a group of nodes, using the same network level message passing functions. This service extends to enable the loading of multiple processes across groups of compute nodes in the system.

Name Server Services

Independence from topology is further enhanced by a facility commonly referred to as a Name Server. Processes, at arbitrary locations on the network, have the ability to register themselves with *GENESYS* by passing an argument (ASCII string) which is unique to that process (e.g. "frame_buffer"). Other processes which may wish to send to that process can determine its location by interrogating *GENESYS* which will return the necessary information to enable communication to take place.

3.2 Process Management

GENESYS processes can run either on the host or on compute nodes. A *GENESYS* process on the host is also a UNIX process, and can access any service provided by UNIX as well as most *GENESYS* services. Process management of host processes uses the usual UNIX facilities, and is not discussed here.

Compute Node Processes

Many processes can be active at once on each compute node. All processes that are ready to run, that is, not *blocked* waiting for a message or signal, are allowed to run in an order controlled by their priority. Priorities can be chosen to allow the order of (non pre-emptive) scheduling to be completely controlled, making *GENESYS* suitable for many soft real time applications.

Each process has a text area containing the code of the process, which can be shared with other instances of the process on the same node, two data areas which are set aside for initialised and uninitialised data, and a stack. The size of the stack is specified when the process is started, and is fixed for the lifetime of the process.

For the transputer, if the stack requirements of a process are sufficiently small, *GENESYS* can place the stack in faster on-chip memory.

Process scheduling

All user processes have a *GENESYS* priority (a non-negative integer specified when initialising). Processes are started with a zero priority, but this can be changed by the process at any time. A process with zero priority is scheduled to run whenever it is not blocked. If more than one is ready to run, they are run in a round-robin fashion.

If more than one process with a non-zero priority is ready to run, then only the process with the highest priority will be permitted to execute. It will run until it blocks, or until it makes a call to the local kernel[1] and another higher priority process is waiting to run.

On transputer based compute nodes, all user processes run at low transputer priority. *GENESYS* processes with zero *GENESYS* priority are executed in turn using the transputer hardware support for this.

Process creation

Processes can be created from executable files on the host file system or by replicating an existing process to form a new process on the same node or any other node. A single process can start new threads of control, each with its own stack, to execute in parallel with the original.

3.3 Other Operating System Services

File system

The file system of the host can be accessed from any node. Libraries of UNIX compatible routines are supplied so that program source can remain unchanged. Four types of access to the file system are available:

- Unbuffered synchronous and asynchronous I/O
- Buffered I/O
- I/O to a memory ("scratch") file

I/O to memory files is useful for applications requiring high speed access to temporary or pre-loaded data.

Signals

Programs running on the host can use UNIX signals. All *GENESYS* programs, both on the host and on compute nodes, can use the *GENESYS* signal package. Signals can be sent from one process to another, caught, ignored or blocked. A signal is received by a process on the next kernel call (most *GENESYS* calls involve a kernel call), and that kernel call can be automatically retried if desired.

Networking Host Nodes

GENESYS currently enables a single host node to be utilized as part of the parallel system. However, this does not have to be directly connected to the compute nodes. It could be a computer at some other location.

GENESYS allows any computer (currently only Sun workstations) which is connected to the network and supports NFS (Network File

1. As part of the run-time system running on each compute node, a kernel process is used to enable synchronization between application processes and other run-time services.

System) together with sockets (or some network communication capability) to be used as the host node. In this way, users having logged in to their local Sun workstation can access the resources of the compute nodes remotely. The file system made available to the compute nodes will be that of the users local computer.

Where there are sufficient quantities of compute nodes, it is possible to introduce the concept of the computational resource server. A single computer on the network "front ends" the compute nodes making them available for use from the rest of the network. Users then log into their local computer and utilize the required portion of the compute nodes remotely.

4 Development Tools

The *GENESYS* development environment is based on that of UNIX. Where possible, the UNIX tools, such as editors and source control programs, are used. *GENESYS* tools are modelled on those of UNIX, performing equivalent operations in similar ways and accepting many of the same options.

GENESYS provides ways of accessing many UNIX services, such as the file system, from all nodes. In other cases, such as the C math library, *GENESYS* provides equivalents to the UNIX service which provide the same functionality in the same way.

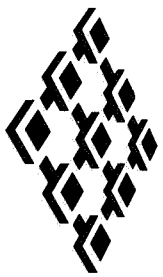
This approach permits the UNIX programmer to become quickly productive since only the areas which are unavoidably different from UNIX need be learnt. Many existing programs can be compiled without change to run under *GENESYS*. A program that runs on a compute node usually needs only minor changes to run on the host, consisting mostly of a single call to inform *GENESYS* that this process is a *GENESYS* process.

4.1 Programming Tools

Compilers

Compute node programs are written with the *GENESYS* ANSI standard FORTRAN or C compilers. Each supports a full implementation of the language, together with a complete set of standard library routines. Further libraries are also provided to access *GENESYS* services, or to provide equivalents to common packages such as the C math library.

The compilers have options to control the placement of data, the evaluation of floating point expressions, to include code that checks for stack overflow, or to include information for the *GENESYS* source level debugger.



Source level debugger

The *GENESYS* source level symbolic debugger (*tdb*) together with its windowed interface (*tdbtool*) provides breakpoints, source listings, data alteration and examination using C expressions with symbolic names (see Figure 6). Any process on any compute node can be debugged, if compiled with the appropriate options, and several copies of the debugger can run simultaneously, allowing the debugging of multiple process on the same or different nodes.

To enable independence of topology, the tdb debugger utilizes the network level communication services of *GENESYS*. Any process on any node can be debugged at the source level.

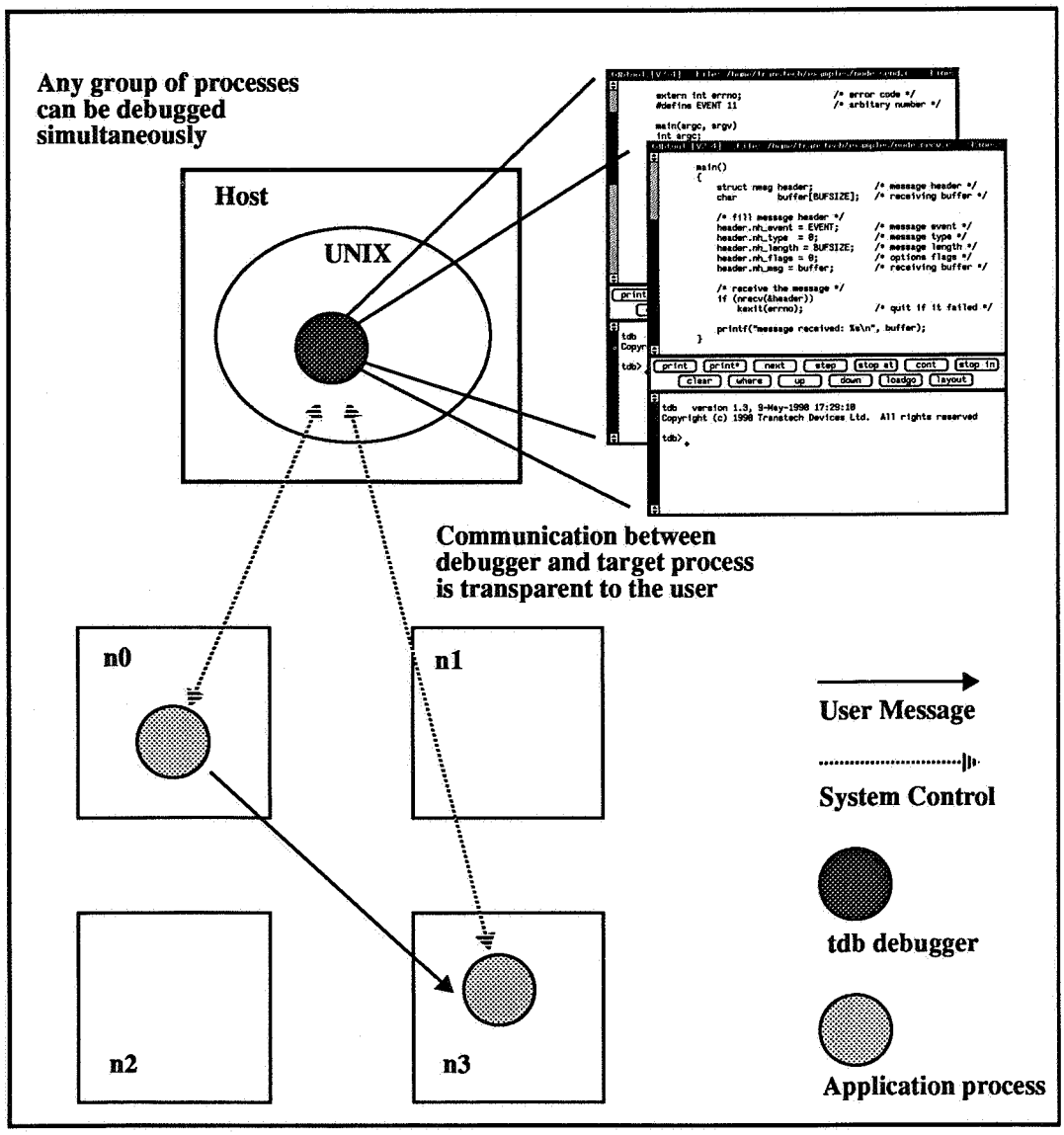


Figure 6 Source Level Symbolic Debugger

Performance Monitors

GENESYS provides a performance monitoring service which is capable of extracting some of the "vital statistics" of the parallel system. These include processor activity (based on idle time measurements) and message transfer activity across transputer links. This information is fed to the host node where it can be stored in data files or displayed graphically.

Other tools

Other tools provided include an assembler and linker, and tools to construct libraries from *GENESYS* object files.

5 Using *GENESYS*

GENESYS is capable of supporting any processor topology capable of allowing direct or indirect communication via message passing between processing nodes.

5.1 Configuring *GENESYS*

The configuration of a *GENESYS* system is controlled by two schemata: the Boot Schema, which specifies the nodes, their connections and types, and the Process Schema, which gives the processes to start when booting *GENESYS* on each type of node. The Boot Schema, for example, enables each compute node in the system to be given an arbitrary number which is then used as the label (or address) for that node, to be used by programs running under *GENESYS* needing to send messages or access the services of that node.

GENESYS can extend to run across arbitrary arrays of compute nodes, some of which could be part of the users own proprietary hardware system.

The routing of messages is given by tables loaded into each node when it is booted. Normally these routes are automatically constructed using the link information of the Boot Schema, but the Boot Schema can contain explicit routes for some or all possible paths if the application has particular requirements.

The *GENESYS* system processes are listed in the Process Schema. Application processes can also be included here if considered necessary. If, for example, an application does not require dynamic process creation, then starting the processes here means that several *GENESYS* system processes are no longer needed, leaving the maximum amount of memory free for the application.

5.2 Monitoring and Controlling *GENESYS*

Many features of *GENESYS* can be examined or altered using *GENESYS* commands. These commands can be used like any standard UNIX command, for example from the shell command line. The services provided by these commands include:

- monitoring of memory allocation
- starting and terminating processes
- configuring the buffering of messages

All the functions used by the commands are directly available to the programmer, so custom commands for particular applications can easily be written.

6 Conclusion

The services provided by *GENESYS* support the application developer who, in turn, becomes free to concentrate on application specific areas.

By concentrating on providing only what it can do best, *GENESYS* is the bridge between the standard UNIX host and the powerful computing capacity of the network of compute nodes.

The simple but powerful message passing and flexible process management facilities of *GENESYS*, enables a suitable hardware independent development environment for today's processors as well as those of tomorrow.

7 References

[1] TTM100: An i860 Processing Unit for Multi-Processing Systems, Transtech Technical Note No. 1, S.J.Bradshaw, May 1990.

8 Bibliography

[1] *GENESYS* Command Reference Manual.

[2] *GENESYS* FORTRAN Reference Manual.

[3] *GENESYS* C Reference Manual.

[4] *GENESYS* User Guide.

[5] A *GENESYS* Tutorial.

NOTES

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TTM100: An i860 Processing Unit for Multi-Processing Systems

S.J.Bradshaw

Transtech Technical Note, No. 1.
May 1990.

TRANSTECH

parallel
technology

Company Profile

Transtech was formed in March 1986 as the research, government establishment and education agent for INMOS transputer based products. The portfolio was quickly expanded to include systems from the key parallel processing start-ups. Commitment to customer support and service, backed by an expert technical team, has driven Transtech's growth and it is now recognised as the world's leading transputer supplier. Already a major manufacturer, Transtech has led the development of open systems for both parallel processing hardware and software; this proven on a growing family of host enviroments.

Transtech has built dedicated sales and customer service teams, these being experienced people in both the commercial and technical requirements of supporting high performance systems. Combining these skills with a well developed contact and information database has given much to Transtech's reputation for satisfying customer demand. Transtech is used to supporting OEM and VAR customers as well as end users.

Transtech supports the most comprehensive range of transputer systems, focusing on high performance and superior functionality at sensible cost. In particular, Transtech has led the marketplace in transputer module and motherboard development. Transtech now boasts three extensive ranges of transputer module products: generic, high performance, and application specific. Motherboards are available for PC, PS/2, VME, Sun, Apollo, Macintosh and stand-alone systems. Transtech also boasts the worlds largest installed base of Sun hosted transputer systems, complemented with its own high performance compilers and Operating System GENESYS.

1 Introduction

The TTM100, an i860 based transputer module, has been developed to offer the many advantages of high performance vector processing to the transputer based parallel processing community. Intel's new and revolutionary i860 processor is used to deliver up to 80MFLOPS of vector based computational performance alongside the most recent of the Inmos transputers, the T805.

A comprehensive suite of industry standard scientific, vector, and signal processing libraries enable the computational capabilities of the i860 to be easily exploited. Each TTM100 is provided with an initial suite of over 250 such routines. Additional packages focus on particular applications, examples of which include Linear Algebra and Image Processing. In total, over 1000 routines can be utilized with the TTM100.

The TTM100 is ideal for parallel applications which are computationally intensive and require performance greater than that available from transputers. Applications particularly suited include:

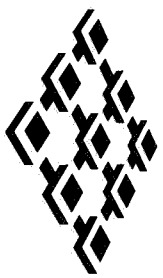
- Signal and Image Processing
- Seismic Exploration
- Computational Physics and Chemistry
- Finite Element Analysis
- Computational Fluid Dynamics
- Any other areas with significant levels of vector and/or matrix manipulation requirements.

2 The TTM100 i860 transputer Module (TRAM)

The TTM100 (see Figure 1:) contains an i860 vector processor clocked at 40MHz, a T805 transputer clocked at 25MHz, 4 (or 16) MBytes of fast page mode dynamic RAM and 1 (or 4) MBytes of dynamic RAM accessible only to the T805 transputer.

The TTM100 has been designed to conform to the now industry standard for transputer modules (see [1]). A TRAM is a self contained processing element which conforms to physical dimension, interface, and hardware interconnection specifications. Measuring only 164mm by 93mm (size 6 in TRAM terminology) the TTM100 can be used with any system capable of utilizing that standard.

The TRAM approach is excellent for maintaining independence and portability between different host environments and interfaces. It is also the most frequently used standard for transputer systems and is adopted by more than 15 manufacturers worldwide.



As a result, the TTM100 is suitable for use with a wide range of TRAM Motherboards in a variety of hardware environments ranging from stand-alone and PC-AT Bus configurations to VME/Sun hosted systems. It is compatible with and can be plugged on to any TRAM motherboard conforming to the TRAM standard.

2.1 Communication with other transputers

The TTM100 communicates with other processing units using four 20 MBits/s bidirectional transputer links. It is also capable of controlling other TRAMs and other transputer based systems using its sub-system port.

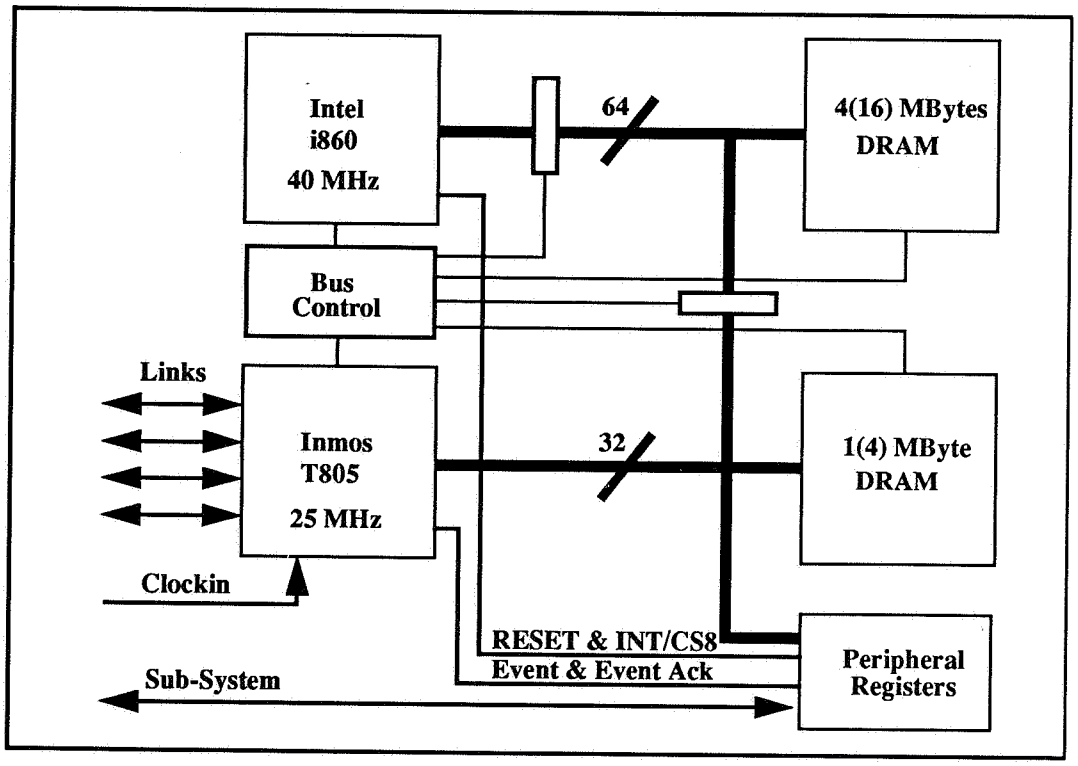


Figure 1: TTM100 incorporating Intel i860 vector processor

3 The i860 Vector Processor

The Intel i860 (see [2]) was designed for numerically and vector intensive applications. Many of the design principles used have been adopted from supercomputer technology enabling the i860 to deliver a peak arithmetic performance of 80 MFLOPS (single precision) and 60 MFLOPS (double precision) in conjunction with a peak integer performance of 40MIPS. In particular, its high throughput is achieved from a combination of RISC design techniques, pipelined processing units, wide data paths, and large on-chip caches.

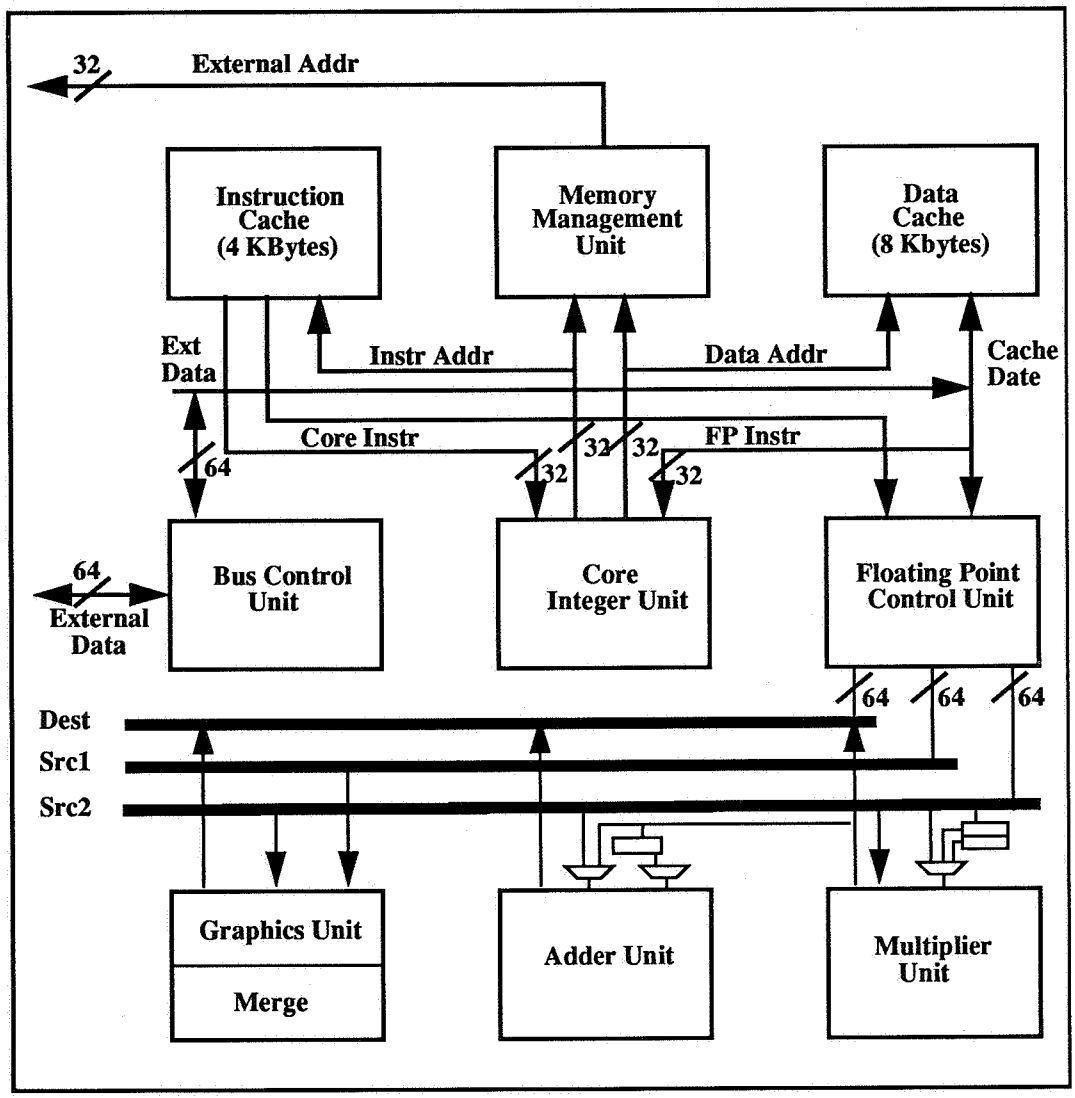


Figure 2: Block Diagram of i860 Microprocessor

Implemented on a single chip with over 1,000,000 transistors, the i860 supports a 64-bit architecture and is capable of executing up to three operations each clock cycle (25ns @ 40MHz). On a single chip, the architecture supports the following facilities:

- Integer Operations
- Floating Point Operations
- Graphics Operations
- Memory-management support
- Data Cache and Instruction Cache

The ability to provide all of these facilities, all on the same silicon, enables hardware developers to create products which are less

dependent on the many external components normally associated with sophisticated computer systems; from this point of view the i860 is similar to the transputer. The i860 is an ideal candidate for integration into highly parallel computer environments: high computational performance, modularity, and low real-estate requirements.

3.1 Core Execution Unit

The i860 is centrally controlled by the (Integer) Core Unit. It is responsible for fetching both integer and floating point instructions and decoding and executing integer, logical, control-transfer, load/store, exception handling, and cache flushing instructions. Instructions are fetched into the core execution unit from the instruction cache. If an address location is not in the cache (a cache miss), the instruction is fed to the core execution unit from external memory, while the corresponding Instruction Cache block is simultaneously filled.

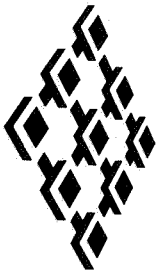
The Core Unit uses a pipeline organization and has been designed according to RISC principles to maximize performance; instructions are purposefully simple and appear to operate in one clock cycle. Furthermore, the use of register bypassing and score-boarding techniques allow the load and store instructions to be executed at a sustained rate of one instruction every clock cycle, assuming that data and instructions are found in their respective caches. At this rate, the Integer Core Unit delivers 40 MIPs of native integer operation performance when executing with a 40MHz clock.

3.2 Floating Point Unit

The Floating Point Unit contains a control unit, an adder, and a multiplier unit. Operations can be executed in scalar or pipeline mode in the adder and in pipeline mode in the multiplier. In scalar mode, new operations are not started until the previous ones are completed. In pipelined mode up to three instructions can be overlapped and executed concurrently at any one time in the adder (see Figure 3:) and two in the multiplier.

With the support of the Instruction and Data Caches, the Floating Point Unit is capable of executing two single precision floating point operations, one add and one multiply, every clock cycle; this is equivalent to 80MFLOPS with a 40MHz clock. An efficient implementation of multiply-accumulate operations makes the i860 well suited for a wide range of numerically intensive application areas including:

- matrix manipulation (e.g., solving linear equations)
- series calculations (e.g., expansion series)
- signal processing calculations (e.g., Fast Fourier Transforms)
- graphics (e.g., coordinate transformations)



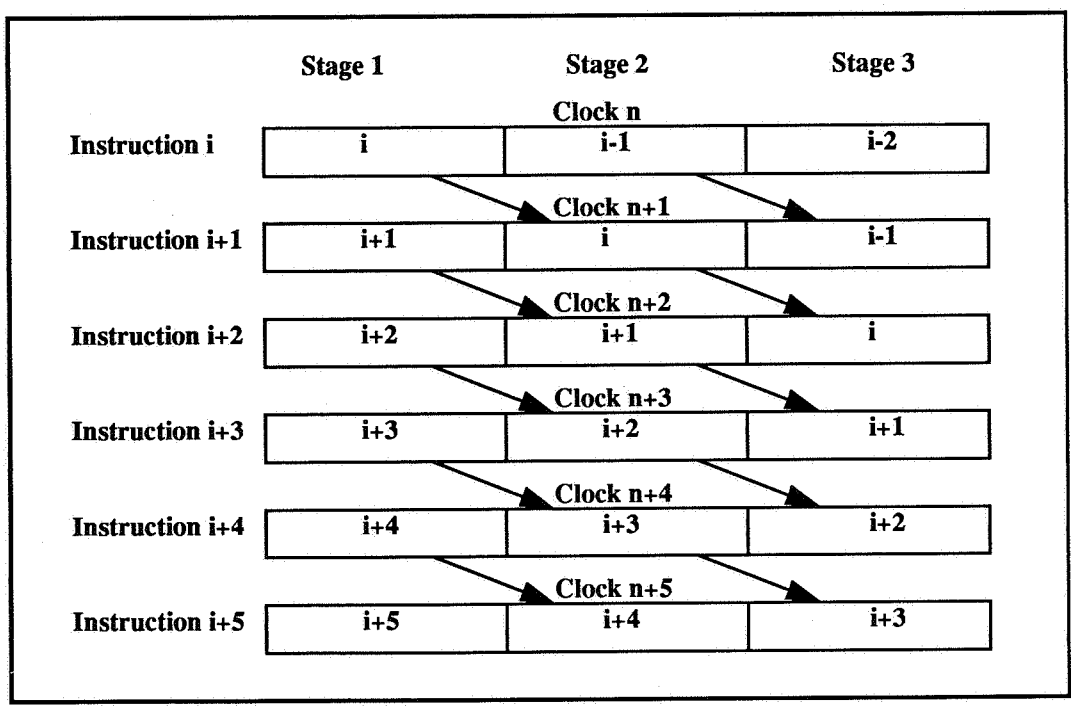


Figure 3: Pipelined Instruction Execution in FPU

Floating-point data types, floating-point instructions, and exception handling all support the IEEE standard for binary floating point arithmetic (see [4]) for both single- and double-precision data types. A complete set of traps includes tests for invalid source operands such as NaN (Not a Number), denormalized numbers, and infinities, as well as tests for errors in the result such as overflow and underflow.

4 Operation of the TTM100

The TTM100 enables both processors to execute concurrently and independently. Memory is split in to two autonomous sections, local, private memory for the transputer and globally accessible system memory for the i860.

4.1 Memory Utilization

The transputer executes its code on the 1 (or 4) MBytes of private memory which is inaccessible to the i860. The private memory address map is identical to that of the more primitive T800 and T801 based transputer modules available from Transtech and other companies.

The i860 utilizes the 4 (or 16) MBytes of system memory which is globally accessible to both processors; a portion of this memory is used to support inter-processor communications. The page mode capability of

the i860 is used to provide faster memory access (zero wait state) when sequential reads or writes take place; this occurs during cache updates for example.

The system memory interface optimizes block move transfers between private and system memory invoked by the transputer. Access to the system memory is based on a fair arbitration mechanism and prevents both processors from reading and/or writing to the shared memory at the same time.

4.2 Peripheral Registers

Peripheral registers are provided to support software driven interrupts for inter-processor communication and the TRAM sub-system port for controlling other transputer based resources.

4.3 Inter-Processor Message Passing

Although transparent to most users, low level message passing between the i860 and transputer is a service which all applications rely on. The message passing system is based on the use of software interrupts which are asserted from either processor by setting the appropriate peripheral registers.

The registers are accessible to both processors and either processor is capable of interrupting the other. Which processor performs the role of 'master' is entirely dependent on the software being used. i.e. the i860 can be used as a co-processor to the transputer or the transputer can be used as a communications sub-system for the i860.

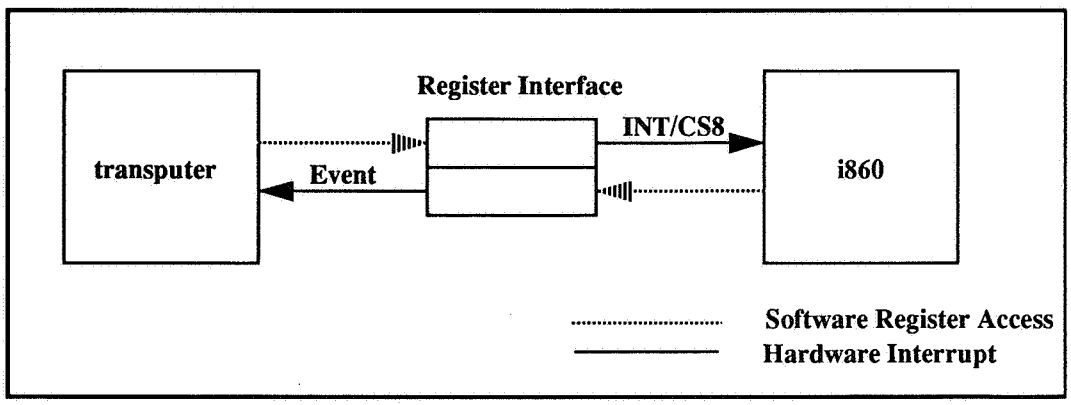


Figure 4: Asynchronous Processor Interrupt Mechanism

Developers utilizing one of the i860 vector libraries, for example, will observe that this service is implemented transparently. Calls to the vector subroutines on the transputer result in the i860 automatically executing the appropriate task.

4.4 Sub-System Services Control

The subsystem reset, analyze and error signals are available but can only be accessed by the transputer. i.e. regardless of which mode the TTM100 is used, the transputer is always responsible for communications and control of other transputer based hardware.

4.5 Booting the TTM100

The T805 is used to boot the i860 by holding the i860 in reset whilst loading the memory with bootstrap code. Upon resetting the TRAM, the transputer is reset in the normal manner but the i860 is held in reset by the hardware, with HOLD asserted, releasing the bus to the transputer. The i860 code is then written to the boot address in the System RAM by the transputer before the i860 is released from reset by the transputer

5 Software Integration

The TTM100 can be integrated into existing transputer environments and will execute existing transputer software without modification. Utilization of the many subroutine and function libraries enables the i860 to be treated as an embedded vector or array processor. No additional programming effort is required. Users can select from a wide range of libraries which are either provided with the TTM100 or available as options. Of the library packages available, many conform to industry and de-facto standards such as those laid down by the Society of Exploration and Geophysics (SEG) or have been established at Research Laboratories such as Lawrence Livermore.

Support is also provided for developers wishing to access and utilize the i860 directly. An array of communication and synchronization libraries enable the i860 to utilize the transputer as its communication system.

5.1 Generic Scientific Libraries

A range of over 250 (single and double precision) generic scientific/vector libraries are provided with each TTM100. Once loaded on the i860, they can be called from any language on the transputer, providing a straightforward and easy to use mechanism for utilizing the i860's resources. The libraries cover the following areas:

- Real/Integer Vectors
- Complex Vectors
- Matrices
- Signal & Image Processing
- BLAS (level 1)

The following diagram indicates how these libraries can be utilized from FORTRAN running under the GENESYS II Operating System.

```
C
C     This program multiplies the elements of two vectors, A and B.
C
      INTEGER IA, IB, IC, LEN
      REAL A(6), B(6), C(6)
C
      DATA IA, IB, IC, LEN / 1, 1, 1, 6 /
      DATA A / 1.0, 2.0, 3.0, 4.0, 5.0, 6.0 /
      DATA B / 3.0, 2.0, 1.0, 1.0, 2.0, 3.0 /
C
C     VECTOR MULTIPLY C(i) = A(i) * B(i)
      CALL VMUL(A, IA, B, IB, C, IC, LEN)
C
      WRITE (*,100) C
100   FORMAT (3X, 'C(i) RESULTS : ', 6F8.2)
C
      END
```

Figure 5: FORTRAN code example of vector library call

5.2 Optional Libraries

In addition to the generic libraries mentioned, Transtech can provide a number of optional packages for the TTM100:

- Hand coded Scientific/Vector Library (high performance)
- Linear Equation Solvers
- High Performance BLAS
- Image Processing

Further information on these libraries can be obtained by contacting Transtech directly.

DOTPR	Dot Product
LVEQ	Logical vector equal
LVGE	Logical vector greater than or equal
LVLE	Logical vector less than or equal
LVLT	Logical vector less than
LVNE	Logical vector not equal
LVNOT	Logical vector not
MAXMGV	Maximum magnitude element of a vector
MAXV	Maximum element of a vector
MEAMGV	Mean of vector element magnitudes
MEANV	Mean value of vector elements
MEASQV	Mean of vector element squares
MINMGV	Minimum magnitude of an element
MINV	Minimum element of a vector
MLINFT	Multi-linear regression
MVESSQ	Mean of vector element singed squares
POLYFT	Polynomial regression
PSORT	Partial sort
RMSQV	Root mean square of vector elements
SPLBAP	Bicubic spline approximation
SPLBIN	Bicubic spline interpolation
SPLCAP	Cubic spline approximation
SPLCIN	Cubic spline interpolation
SSMEAN	Sum of squares (from the mean)
SVDIV	Scalar vector divide
SVE	Sum of vector elements
SVEMG	Sum of vector element magnitudes
SVESQ	Sum of vector element squares
SVESSQ	Sum of vector element signed squares
VAAM	Vector add, add multiply
VABS	Vector absolute value
VADD	Vector add
VAM	Vector add and multiply
VASBM	Vector add, subtract, multiply
VASM	Vector add and scalar multiply
VATAN	Vector arctangent
VATAN2	Vector arctangent (2 arguments)
VCLIP	Vector clip
VCLR	Vector clear
VCMPRS	Vector compress
VCOS	Vector cosine
VDIV	Vector divide
VDIVZ	Vector divide with zero test
VEXP	Vector exponential
VECP10	Vector exponential (base 10)
VFILL	Vector fill with constant
VFLOAT	Vector float to real
VFRAC	Vector truncate to fraction
VGATHR	Vector gather
VGEN	Vector generate
VICLIP	Vector inverted clip
VIFIX	Vector fix to integer
VINDEX	Vector index
VINT	Vector truncate to whole number
VINTB	Vector interpolate between vectors
VLIM	Vector limit
VLINT	Vector linear interpolation
VLMERG	Vector logical merge
VLOG	Vector logarithm (natural)
VLOGGM	Vector log-gamma
VMA	Vector multiply and add
VMAX	Vector maximum of two vectors
VMAXMG	Vector maximum magnitude of two vectors
VMIN	Vector minimum of two vectors
VMINMG	Vector minimum magnitude of two vectors
VMMA	Vector multiply, multiply, add
VMMSB	Vector multiply, multiply, subtract
VMOV	Vector move
VMSA	Vector multiply and scalar add
VMSB	Vector multiply and subtract
VMUL	Vector multiply
VNABS	Vector negative absolute value
VNEG	Vector negate
VPOLY	Vector polynomial evaluation
VPYTHAG	Vector pythagoras
VQINT	Vector quadratic interpolation
VRAMP	Vector fill with ramp
VRAND	Vector random number generator
VRANDN	Vector normally distributed random number generator
VRECIP	Vector reciprocal
VRVRS	Vector reverse ordering
VSADD	Vector scalar add
VSBM	Vector subtract and multiply
VSBSBM	Vector subtract, subtract multiply
VSBSM	Vector subtract and scalar multiply
VSCATR	Vector scatter
VSDIV	Vector scalar divide
VSIMPS	Simpson integration
VSIN	Vector sine
VSMSA	Vector scalar multiply and scalar add
VSMSB	Vector scalar multiply and subtract
VSMUL	Vector scalar multiply
VSOCFX	Vector scale, offset, clip, and fix to integer
VSQ	Vector square
VSQRT	Vector square root
VSQRTZ	Vector square root with zero test
VSSQ	Vector signed squares
VSUB	Vector subtract
VSUM	Running sum integration
VSWAP	Vector swap
VTAN	Vector tangent
VTHR	Vector threshold
VTMERG	Tapered merge of two vectors
VTRAPZ	Trapezoidal integration
ZRFUNC	Zeros of a function
ZRPOLY	Zeros of a polynomial

Figure 6: Basic Operations for Real/Integer Vectors

CDOTPR	Complex dot product
CRVADD	Complex and real vector add
CRVDIV	Complex and real vector divide
CRVMUL	Complex and real vector multiply
CRVSUB	Complex and real vector subtract
CVABS	Complex vector absolute
CVADD	Complex vector add
CVCOMB	Complex vector combine
CVCONJ	Complex vector conjugate
CVDIV	Complex vector divide
CVEXP	Complex vector exponential
CVFILL	Complex vector fill
CVMA	Complex vector multiply and add
CVMAGS	Complex vector magnitude squared
CVMEXP	Complex vector multiply exponential
CVMGSA	Complex vector magnitude squared and add
CVMOV	Complex vector move
CVMUL	Complex vector multiply
CVNEG	Complex vector negate
CVPHAS	Complex vector phase
CVRCIP	Complex vector reciprocal
CVREAL	Form complex vector from reals
CVSMUL	Complex vector scalar multiply
CVSQRT	Complex vector square root
CVSUB	Complex vector subtract
POLAR	Rectangular to polar conversion
RECT	Polar to rectangular conversion
VIMAG	Extract imaginaries of complex vector
VREAL	Extract reals of complex vector

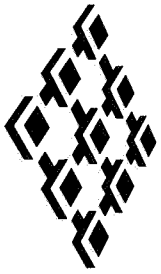
Figure 7: Basic Operations for Complex Vectors

CGEAA	Complex general matrix eigensystem, all values, all vectors
CHEAA	Complex hermitian matrix eigensystem, all values, all vectors
CMES	Complex matrix, envelope symmetric
CMESFC	Complex matrix, envelope, symmetric factor
CMESFS	Complex matrix, envelope, symmetric factor and solve
CMESSV	Complex matrix, envelope, symmetric solve
CMFUFC	Complex matrix, full, unsymmetric factor
CMFUFS	Complex matrix, full, unsymmetric factor and solve
CMFUIN	Complex matrix, full, unsymmetric invert
CMFUSV	Complex matrix, full, unsymmetric solve
CMMUL	Complex matrix multiply
CMMULG	Complex matrix multiply (generalized version)
CMMULS	Complex submatrix multiply
CMSS	Complex matrix, sparse, symmetric reorder/factor/solve
CMSSFC	Complex matrix, sparse, symmetric factor
CMSSFL	Complex matrix, sparse, symmetric fill in
CMSSFS	Complex matrix, sparse, symmetric factor and solve
CMSSSV	Complex matrix, sparse, symmetric solve
CMSU	Complex matrix, sparse, unsymmetric
SMSUFC	Complex matrix, sparse, unsymmetric factor
SMSUFL	Complex matrix, sparse, unsymmetric factor
SMSUFS	Complex matrix, sparse, unsymmetric factor and solve
SMSUSV	Complex matrix, sparse, unsymmetric solve
CMTRAN	Complex matrix transpose
CMTUFC	Complex matrix tridiagonal unsymmetric factor
CMTUFS	Complex matrix tridiagonal unsymmetric factor and solve
CMTUSV	Complex matrix tridiagonal unsymmetric solve
CNDOTP	Complex nested dot product
MORMD	Matrix minimum degree reordering
MORRCM	Matrix reverse Cuthill-McKee reordering
RGEAA	Real general matrix eigensystem, all values, all vectors
RMES	Real matrix, envelope, symmetric reorder/factor/solve
RMSS	Real matrix, sparse, symmetric reorder/factor/solve
RMSU	Real matrix, sparse, unsymmetric reorder/factor/solve
RMESFC	Real matrix, envelope, symmetric factor
RMESFS	Real matrix, envelope, symmetric factor and solve
RMESSV	Real matrix, envelope, symmetric solve
RMFUFC	Real matrix, full, unsymmetric factor
RMFUFS	Real matrix, full, unsymmetric factor and solve
RMFUIN	Real matrix, full, unsymmetric invert
RMFUSV	Real matrix, full, unsymmetric solve
RMMUL	Real matrix multiply
RMMULG	Real matrix multiply (generalized version)
RMMULS	Real submatrix multiply
RMSSFC	Real matrix, sparse, symmetric factor
RMSSFS	Real matrix, sparse, symmetric factor and solve
RMSSSV	Real matrix, sparse, symmetric solve
RMSUFC	Real matrix, sparse, unsymmetric factor
RMSUFL	Real matrix, sparse, unsymmetric fill in
RMSUFS	Real matrix, sparse, unsymmetric factor and solve
RMSUFV	Real matrix, sparse, unsymmetric solve
RMTRAN	Real matrix transpose
RMTUFC	Real matrix tridiagonal unsymmetric factor
RMTUFS	Real matrix tridiagonal unsymmetric factor and solve
RMTUSV	Real matrix tridiagonal unsymmetric solve
RNDOTP	Real nested dot product
RSEAA	Real symmetric matrix eigensystem, all values, all vectors

Figure 8: Matrix Operations

ACORF	Auto-correlation (frequency domain)
ACORT	Auto-correlation (time domain)
ASPEC	Accumulating auto-spectrum
BLKMAN	Blackman window multiply
CCORF	Cross-correlation (frequency domain)
CCORT	Cross-correlation (time domain)
CFFT	Complex FFT (in place)
CFFTB	Complex FFT (not in place)
CFFTM	Mixed radix complex FFT
CFFTSC	Complex FFT scale
CFFTX	Complex FFT using SIN/COS tables
COHER	Coherence function
CONV	Convolution and correlation
CSPEC	Accumulating cross-spectrum
DEQ22	Difference equations, 2 poles, 2 zeros
HAMM	Hamming window multiply
HANN	Hanning window multiply
HIST	Histogram
RFFT	Real to complex FFT (in place)
RFFTB	Real to complex FFT (not in place)
RFFTF	Real to complex forward FFT
RFFTI	Real to complex inverse FFT
RFFTM	Mixed radix real FFT
RFFTSC	Real FFT scale and format
RFFTX	Real FFT using SIN/COS tables
TRANS	Transfer function
VAVEXP	Vector exponential averaging
VAVLIN	Vector linear averaging
VDBCON	Vector conversion to dB
VXCS	Vector multiplied by sine and cosine
WIENER	Wiener-Levinson algorithm

Figure 9: Signal Processing Operations



CAXPY	Complex constant times a complex vector plus a vector		value	**SDOT**	Real dot product
CCOPY	Complex vector copy	**ISAMAX**	Index of real element having maximum absolute value	**SNRM2**	Vector euclidean length
CTC	Complex conjugate dot product	**SASUM**	Sum of magnitudes of real vector components	**SROT**	Apply plane rotation
CDOTU	Complex dot product	**SAXPY**	Real constant times a real vector plus a vector	**SROTG**	Setup Givens plane rotation
CSCAL	Complex constant times a complex vector	**SCASUM**	Sum of magnitudes of complex vector components	**SROTM**	Apply modified plane rotation
CSSCAL	Real constant times a complex vector	**SCNRM2**	Complex vector euclidean length	**SROTMG**	Setup modified Givens plane rotation
CSWAP	Complex vector swap	**SCOPY**	Vector copy	**SSCAL**	Real constant times a real vector
ICAMAX	Index of complex element having maximum absolute			**SSWAP**	Vector swap

Figure 10: BLAS (LEVEL -1)

6 References

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