causes an immediate SCM read reference to that relative address and sends the SCM word to the corresponding operand register X1 through X5. Similarly, placing a quantity into address register A6 or A7 causes the word in the corresponding X6 or X7 operand register to be written into that relative address of SCM.

The A0 and X0 registers operate independently of each other and have no connection with SCM. A0 is used as the relative SCM starting address in a block copy operation and for scratch pad or intermediate results.

B REGISTERS

There are eight 18-bit index (B) registers in the CPU. These registers (B0, B1,...,B7) are primarily indexing registers for controlling program execution. Program loop counts may be incremented or decremented in these registers.

Program addresses may be modified on the way to an A register by adding or subtracting B register quantities. The B registers also hold shift counts for pack and normalize operations and the channel number for channel status requests.

B0 always contains positive zero. It can be used as an operand but cannot hold results from instructions.

INSTRUCTION REGISTERS

INSTRUCTION WORD STACK (IWS)

The IWS is a group of twelve 60-bit registers that hold program instruction words for execution. It is essentially a moving window in the program code. The IWS is filled two words ahead of the program address currently being executed. A small program loop of up to ten instruction words may be entirely contained within the IWS. When this happens, the loop may be executed repeatedly without further references to SCM.

When a shift stack condition exists, each rank is cleared and simultaneously entered with information from the next highest order rank. The information in rank one is discarded. New information arriving from SCM is entered in rank 12.

The twelve registers are individually identified by rank. The rank one register contains the oldest data. If the IWS contains sequential program instruction words, the contents of the rank one register corresponds with the lowest storage address in the instruction address stack.

INSTRUCTION ADDRESS STACK

A group of twelve 18-bit address registers are associated with the IWS. These registers, called the instruction address stack (IAS), hold relative SCM program addresses on a one-for-one basis with the program words in the IWS. The rank one register contains the SCM address from which the word in rank one of the IWS was read. All ranks are compared with the current program address. If coincidence occurs for any rank, the corresponding rank in the IWS is sent to the CIW register.

CIW REGISTER

The CIW register is divided into four 15-bit parcels. All four parcels are loaded when an instruction word is read from the IWS. An instruction issues from the CIW register when conditions in the functional units and operating registers are such that the instruction will be executed without conflicting with previously issued instructions. The other parcels are then shifted left in the CIW register by either 15 or 30 bits, depending upon the instruction format.

P REGISTER

The 18-bit program address (P) register contains the current program execution address. It serves as a program address counter and holds the relative SCM address for each program step. (Refer to Appendix B for related information.) P is advanced to the next program step in the following ways.

1. P is advanced by one when an instruction word is sent to the CIW register.
2. P is set to the address specified by a branch instruction. If the instruction is a return jump, (P) + 1 is stored before entering P with the new value to allow a return to the original sequence.
3. P is set to the address specified in the exchange package.

PSD REGISTER

The program status designator (PSD) register is a collection of 18 program status flags. Six of these flags are mode designators and 12 are condition designators. The arrangement of these flags in the register is illustrated in Figure 2-2.

The PSD register is loaded from the exchange package during an exchange jump sequence. All 18 bits are entered in the register at this time. The six mode designators remain unaltered throughout the execution interval for the exchange package. The 12 condition designators may be set by conditions that occur during the execution interval. All flags are stored in the SCM exchange package at the end of the execution interval.

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Duplicate entries in the IWS cause no problems unless an instruction is modified during execution. Since this modification occurs only in SCM and since duplicate entries are merged in a logical sum network, an erroneous instruction may result. Therefore, the IWS should be voided by executing a return jump (01) instruction after instruction modification has been performed.

HOLES IN IWS

Several small program sequences may reside in the IWS at the same time. Program execution may branch back and forth between two such sequences. The execution of the sequence occupying the lower ranks of the IWS may branch in such a way that sequential execution is continued into a program area not loaded into the IWS on the initial pass. When this happens, the next sequential instruction word may be missing in the IWS and no request has been made for it.

This situation is equivalent to a branch out of IWS with no branch instruction involved. As soon as the missing word is detected, the hardware initiates a branch out of stack sequence which allows the program to continue with no loss of information.

EXCHANGE JUMP

The exchange jump is a mechanism for switching between programs.

The execution of an exchange jump involves the simultaneous storing of all pertinent information in the CPU operating registers and control registers into SCM and writing new information from SCM into these same registers. This block of data is called an exchange package. An exchange package (Figure 4-2) provides the following information on a program to be executed.

Program address (P) - 18 bits

Reference address for SCM (RAS) - 18 bits

Field length of program for SCM (FLS) - 18 bits

Reference address for LCM (RAL) - 19 bits

Field length of program for LCM (FLL) - 19 bits

Program status designation register (PSD) - 18 bits

Normal exit address (NEA) - 16 bits

Error exit address (EEA) - 17 bits