Notes of a meeting between participants in the RCO network and ICL, 23rd January 1976

Purpose: The meeting was held to enable ICL to present an updated description of the structure and capabilities of their Communications Network Processor (CNP). ICL were especially concerned about what they believed to be misconceptions in the report 'New Hardware for the 2980 Front End Processor' - TAP/75/64 produced by R.B. Vaughn of ERCC (dated November 1975).

Present: Mr D. Bogie, ICL
Dr G.E. Thomas, ERCC
Mr J.I. Davies, ERCC
Professor S. Michaelson, Department of Computer Science
Dr D. Ellis, ICL
Mr P.E. Williams, ERCC
Mr R.B. Vaughn, ERCC
Mr H. Dewar, Department of Computer Science
Dr. J.G. Burns, ERCC
Mr E. Gaitskell, ICL
Mr C. Jones, ICL
Mr M.P.B. Dolan, ICL
Mr G. Dougan, ICL
Mr J. Robertson, ICL
Mr P.T. Barry, RCO
Mr R. Wickham, RCO

Mr Jones opened the meeting by suggesting an informal agenda. ICL would describe the RCO communications processor requirement and would then show how the Communications Network Processor (CNP) could fulfil it.

Mr Gaitskell outlined the RCO requirements as seen by ICL.

1. 2980 connection
2. Link level control for HDLC
3. Module switching at 'bus' level
4. Line capability

   4 x 48K baud HDLC full duplex
   10 x 9.6K baud BSC
   8 x asynchronous (each up to 9.6K baud)

5. Duplicated System
6. Expansion Capability

The CNP solution offered by ICL appeared immediately to satisfy requirements 1 and 5 above. Requirement 2 would be satisfied by hardware and microcode currently under development.

Mr Vaughn pointed out the ICL standard was for single numbering of HDLC frames but that the RCO network was standardising on double numbering. This sort of difficulty was probably surmountable if it were possible to modify the CNP microcode.

Mr Gaitskell indicated that ICL was capable of satisfying requirement 3 by the development of special hardware to a specific customer requirement. No cost for this was currently available.

Mr Gaitskell questioned the realism of requirement 4 and suggested that no processor currently being offered could meet message rates of several thousand per second which were implied by the line speeds and an average message length of a few tens of characters.

A discussion upon message and character rates to be expected produced the following points. Mr Vaughn made it clear that the figures on the requirement were merely a benchmark against which to judge the performance of various manufacturers' hardware.

The fact that CNP had no direct memory access but took a microprogram interrupt for each character made its capabilities as a character handler somewhat questionable. Mr Gaitskell indicated that the HDLC line unit generated one interrupt per four characters and that the CPU overhead when this took place was 12u sec with current microcode. He pointed out that microcoded character handling allowed the possibility of handling each character only once and leaving the emulated machine to perform only the message by message actions. Dr Burns said that the current EMAS front end processor (a DEC PDP11/45) was handling an average of forty messages per second. It was agreed that although instantaneous character transfer rate might approach the full line capacity described in requirement 4, average message rate would probably not exceed 200-300 messages per second.

Mr Gaitskell indicated that ICL could offer no assurances with respect to requirement 6 since this would involve unacceptable long term commitments.

Mr Vaughn pointed out that his report (TAP/75/64) had raised three other difficulties with respect to the ICL CNP as a RCO communications processor, Firstly, that the ICL position on support for user reprogramming, and in particular re-microprogramming, was unclear. Secondly, that the RCO requirement included provision of stand-alone nodes for use in the general purpose RCO network as well as front-end processing. Thirdly, that ICL did not and probably could not compete with mini computer manufacturers in terms of flexibility and cheapness of additional peripherals. This also extended to a reluctance to provide detailed technical information to allow the attachment of alien hardware.

Mr Gaitskell said that reprogramming the emulated machine was both possible and supported and that a CORAL compiler running on System 4 was available. User access to the microprogram level might be negotiated but no assurance on this could be given. The CNP was designed as a node processor as well as a front-end and this use would be acceptable and supported. ICL could not compete with mini computer manufacturers on the matter of large ranges of cheap peripherals although the provision of information to allow the attachment of alien hardware could be arranged.

Mr Gaitskell went on to describe the CNP system starting with the basic configuration which constituted the CLC multiplexer and the extensions in programming capability and interfacing which made this into a CNP. Two line controllers were available - the NIM1 providing asynchronous and synchronous working up to 9.6K baud producing one interrupt per character and the NIM3 providing HDLC synchronous working up to 9.6K baud and generating one interrupt for every four characters. Only four such HDLC channels could be accommodated on the current back plane.

Dr Thomas requested that this information, and additional information up to the level of detail usually provided by minicomputer manufacturers, be made available to the RCO.

Mr Williams stated the restriction to four HDLC channels on each CNP was likely to prove a fundamental objection to its use as a Node in the RCO network.

Mr Gaitskell gave some details of the CNP processor performance. The average instruction time for the emulated machine would be about 9u seconds. Process switching would require about 24u seconds. The microcode machine had 8 interrupt levels, each with a separate set of registers.

Professor Michaelson asked if the interrupt levels were pre-assigned to particular functions. Mr Gaitskell replied that this was so in the present system but that changes were possible.

Mr Gaitskell stated that the emulated machine/compiler interface was intended to be flexible and that both portability and documentation would be achieved at the CORAL level only. The intention of the design was that all character by character processing, store space management, scheduling, and interrupt handling should take place at the microcode level. Both HDLC channel (NIM3) and mainframe interfaces would work on four bytes at a time. The microcode overhead for HDLC was 12u seconds per four bytes - that is an average of 3u seconds per character. All system generation and compilation facilities at both microcode and emulated machine levels were available currently on System 4 only. The intention was to provide all such facilities on 2900 under VME/B.

Dr. Thomas summed up by saying that the RCO were in the position of looking for a next generation in communications processors with the minimum of preconceived ideas about the structure of such a machine. ICL were attempting to market an existing machine which partook of many of the characteristics of the present generation with a bias towards flexibility of character handling and a corresponding loss in total throughput capability. The aims of the two organisations thus appeared largely incompatible.

Mr Barry observed that the flexibility of the ICL approach was somewhat offset by the higher cost/performance ratio of the CNP relative to its competitors.

Mr Gaitskell indicated that the ICL view was that 7905 and CNP performance was comparable but that 7905 showed a less favourable cost/performance ratio.

Mr Bogie closed the meeting with the hope that a useful exchange of information had taken place despite the somewhat divergent objectives of the two organisations.

J.I. Davies, ERCC

5th February 1976